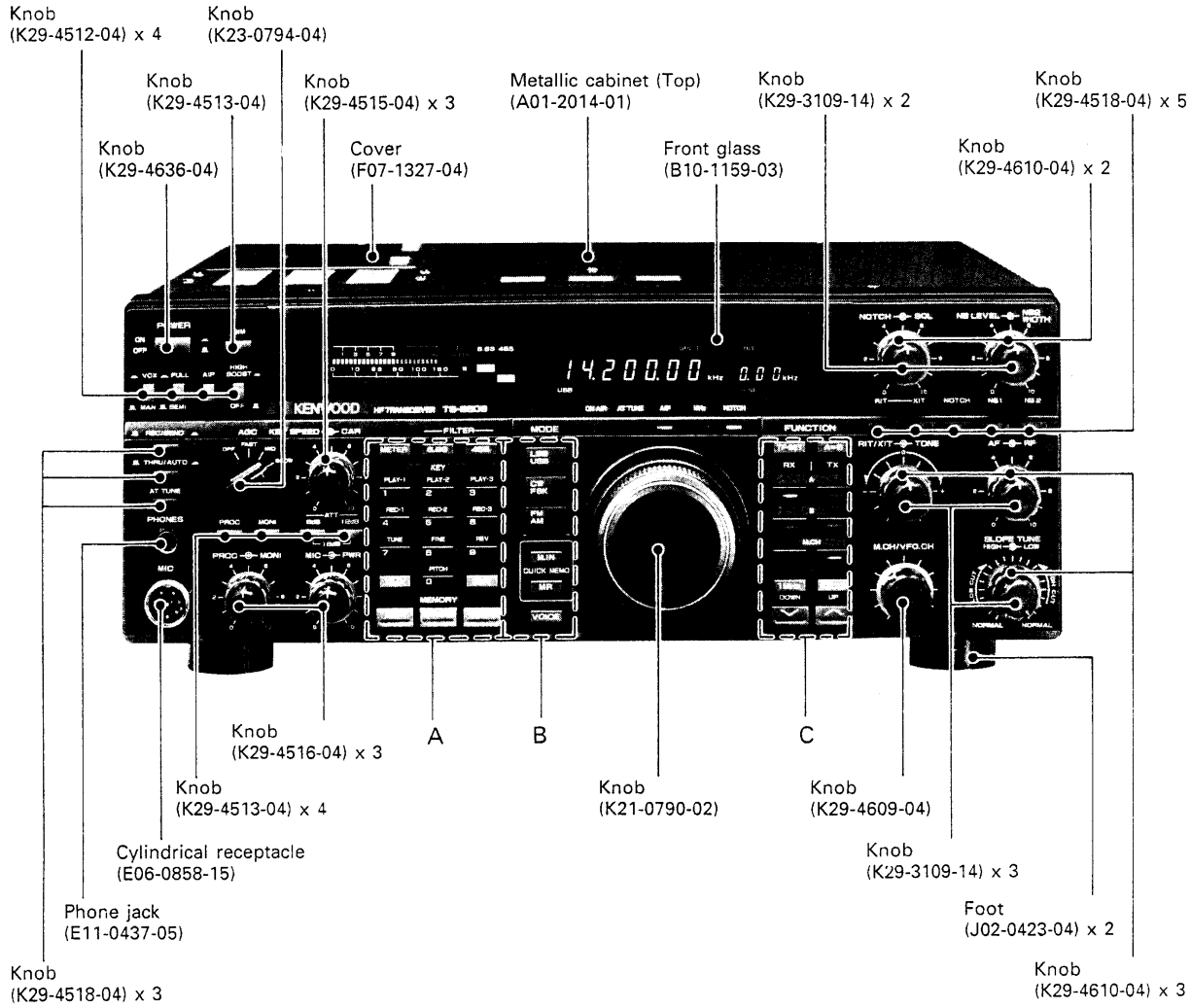
HF TRANSCEIVER

TS-850S

SERVICE MANUAL

TS-850S

KENWOOD



A

Knob (K29-4623-03)	Knob (K29-4624-03)	Knob (K29-4625-03)
Knob (K29-4611-03)	Knob (K29-4612-03)	Knob (K29-4613-03)
Knob (K29-4614-03)	Knob (K29-4615-03)	Knob (K29-4616-03)
Knob (K29-4617-03)	Knob (K29-4618-03)	Knob (K29-4619-03)
Knob (K29-4621-03)	Knob (K29-4620-03)	Knob (K29-4622-03)
Knob (K29-4505-04)	Knob (K29-4506-04)	Knob (K29-4507-04)

B

Knob (K29-4633-03)
Knob (K29-4634-03)
Knob (K29-4635-03)
Knob (K29-4627-03)
Knob (K29-4628-03)
Knob (K29-4626-03)

C

Knob (K29-4631-03)	Knob (K29-4632-03)
Knob (K29-3200-03)	Knob (K29-3200-03)
Knob (K29-3200-03)	Knob (K29-3200-03)
Knob (K29-3200-03)	Knob (K29-3200-03)
Knob (K29-4629-03)	Knob (K29-4630-03)
Knob (K29-4508-04)	Knob (K29-4509-04)

CONTENTS

CIRCUIT DESCRIPTION

Frequency Configuration

The TS-850 utilizes triple conversion in receive mode, double conversion in CW and FM transmit modes, and triple conversion in SSB, AM, and FSK transmit modes.

When the DSP-100 (digital signal processor) is installed, the 36.89-kHz IF (fourth IF) signal goes to the DSP unit during reception; during transmission, the input signal from the microphone or key goes to the DSP unit, and a 455-kHz signal goes to the main unit according to the mode. The DSP only produces a 455-kHz carrier in FM mode, the VCOs operate in the same way as when there is no DSP.

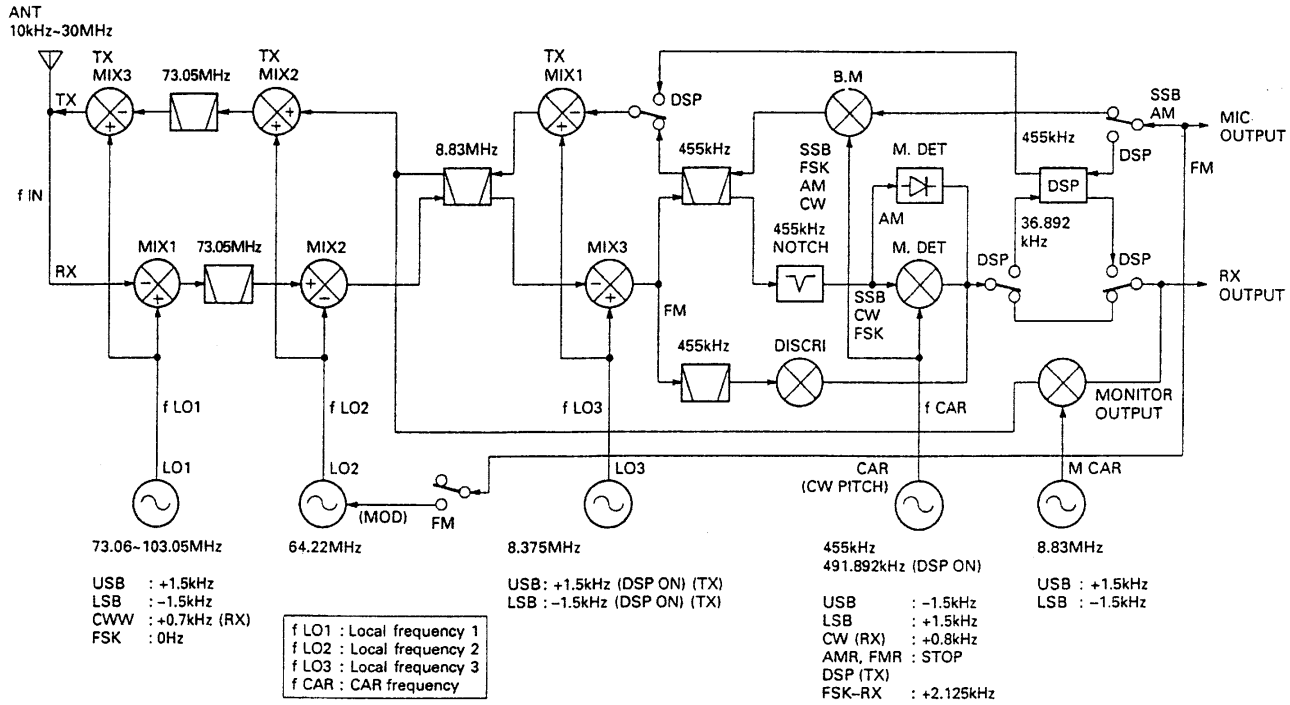


Fig. 1 Signal system frequency configuration

1) Frequency configuration

The receiver frequency in the SSB mode is given by the following equation when the receiver tone produced by the input frequency (f_{IN}) from the antenna is zero beat (when an SSB signal with a carrier point of f_{IN} is zeroed in):

$$f_{IN} = f_{LO1} - f_{LO2} - f_{LO3} - f_{CAR} \ldots\ldots\ldots (1)$$

Since all these frequencies are generated by the DDS (Direct Digital Synthesis) system and the PLL (Phase Locked Loop) circuits (as shown in Fig. 2), the receiver frequency is determined only by the reference f_{STD}, the PLL divide ratio, and DDS data. Therefore, the stability/accuracy of the reference frequency determines the overall frequency stability/accuracy of the transceiver.

The stability/accuracy of the reference crystal oscillator used in the TS-850 is 10 ppm (−10 to +50°C). The stability/accuracy of the optional temperature-compensated crystal oscillator (TCXO, SO-2) is 0.5 ppm (−10 to +50°C).

The TS-850 local oscillator and the CAR DDS circuits are independent of each other. However, they can be operated in a way similar to a "cancel loop" configuration, by changing the CAR and local oscillator data simultaneously by means the microprocessor. This function allows changes in the fcar and f_{LO1} lines when the mode changes, and also allows the bandwidth of the slope tune circuits to be varied (f_{CAR} and f_{LO3}, f_{LO3} and f_{LO1}).

CIRCUIT DESCRIPTION

In the transmit SSB or other modes, the frequency is determined by the reference frequency, (f_{STD}), and the PLL divide ratio. The display frequencies in the various modes are listed in Table 1. (In the FSK mode, the TS-850 displays the mark transmitter frequency.)

The pitch of the incoming signal in the CW mode can be varied without changing the center frequency of the IF filter (variable CW pitch system). Since changes in the receiving pitch are directly related to the sidetone, zero-beating is easily done by receiving the desired signal so that the receiving pitch is the same as the sidetone.

Transmission in the FM mode is carried out by applying the audio signal from the microphone to VCO2 and modulating f_{LO2}.

The CAR signal is stopped by the DSP unit during reception in the AM and FM modes and during transmission. When the DSP unit is connected, f_{CAR} is switched to the signal output from the DSP, and the carrier point is fixed at 455kHz during transmission. Therefore, a shift in the IF frequency is done by f_{LO1} and f_{LO3} by changing the modes.

Since the reference for the DSP is based on f_{STD}, the stability/accuracy of the operating frequency is unchanged even when the DSP is connected.

Mode	Display frequency
USB, LSB	Carrier point frequency
CW	Transmit carrier frequency
FSK	Mark transmit frequency
AM, FM	IF filter center frequency

Table 1 Display frequency in each mode

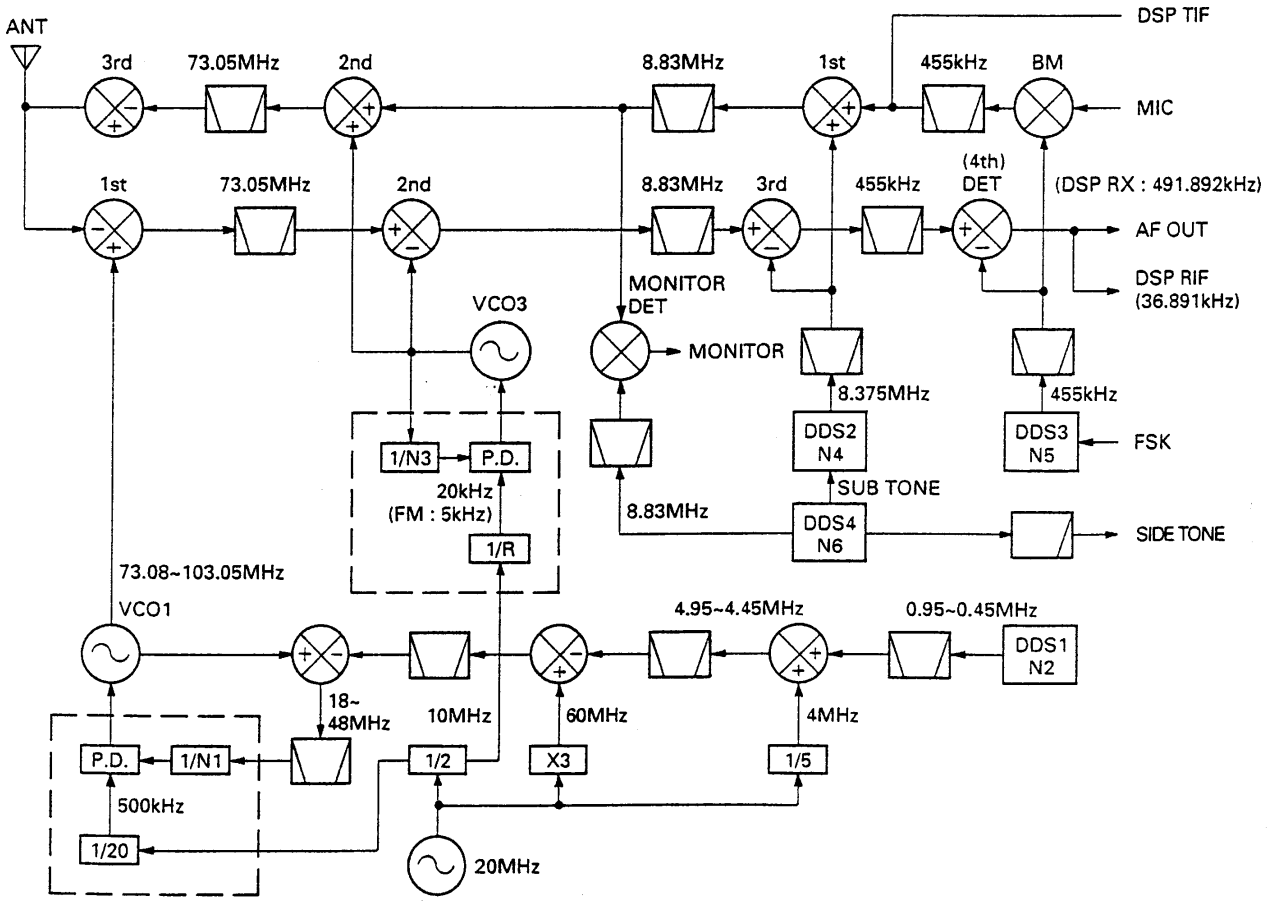


Fig. 2 PLL system frequency configuration

CIRCUIT DESCRIPTION

Local Oscillator Circuit

The TS-850 PLL circuit uses a reference frequency of 20MHz, and consists of a PLL loop which includes the DDS unit, covering 30kHz to 30MHz in 10-Hz or 1-Hz steps, a DDS circuit that generates other local oscillator signals (LO3, MCAR, STON), and a PLL loop that generates LO2. Figure 2 shows the frequency configuration of the local oscillator circuit.

The divide ratio and DDS data to the PLL loop are controlled by the microprocessor, and all the frequencies are based on the reference frequency (fSTD). Figure 3 is the PLL block diagram .

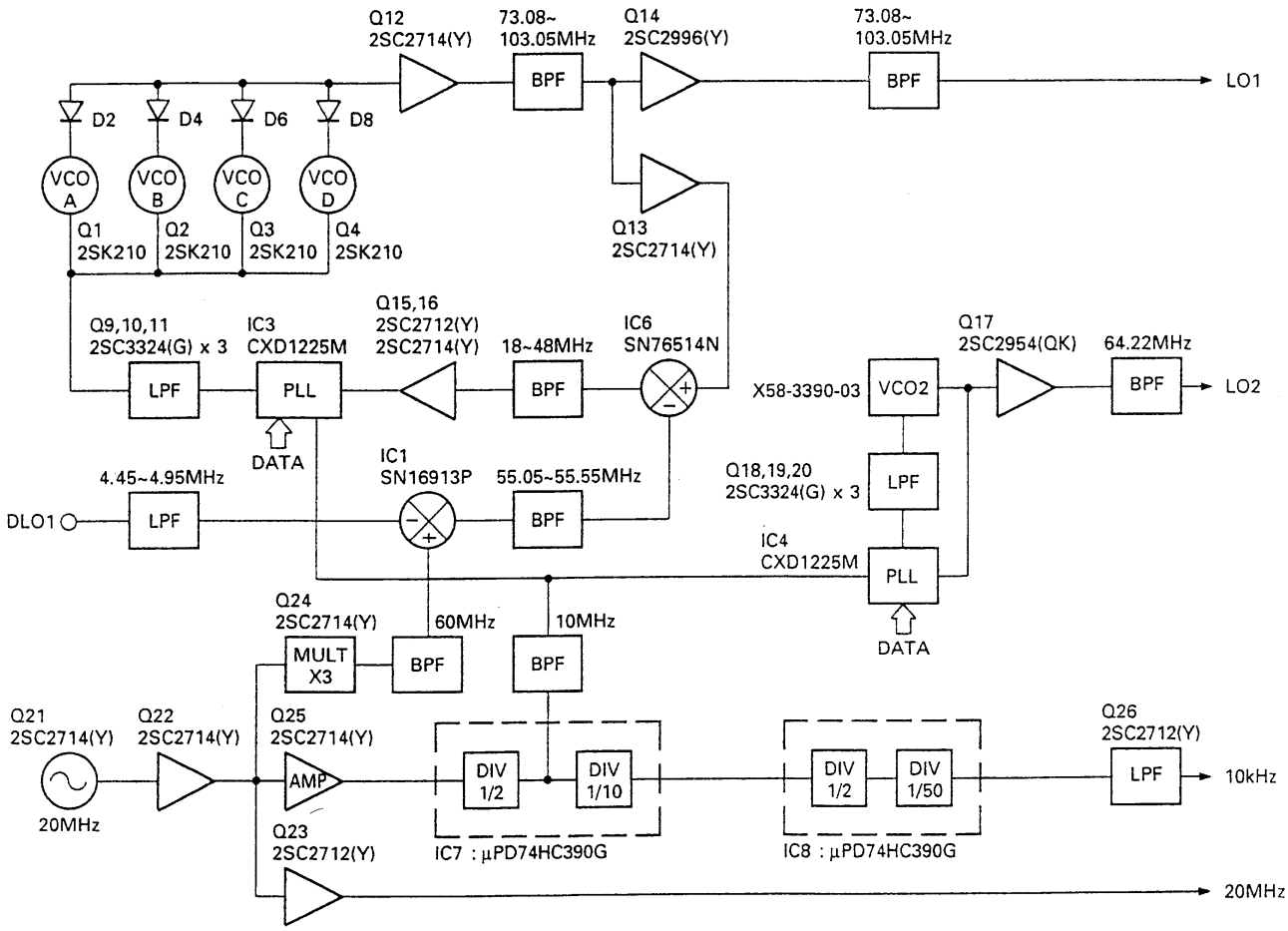


Fig. 3 PLL block diagram

1) Reference oscillator circuit

The reference frequency (fSTD), used for frequency control, is generated by 20-MHz crystal oscillator, X1 and Q21 (2SC2714). Three outputs are provided; one is used as the reference for the CAR unit, the other is divided by three by Q24 to produce a 60-MHz signal, and the other is amplified by Q25, and divided by IC7 and IC8. A 500-kHz marker signal appears at TP5, and the 10-kHz signal passes through the active low-pass filter, Q26, and is output as the reference signal for the external DSP unit. The 10-MHz signal is halved by IC7, and input to IC3 and IC4 (CXD1225M).

The crystal oscillator circuit can be replaced by an optional TCXO (SO-2). The TS-850 can be switched to the TCXO by removing jumper resistors W1 and W2.

CIRCUIT DESCRIPTION

2) LO2

Q1 (2SK508NV) of VCO2 (X58-3390-03) is used to generate a signal of 64.22MHz. The 10-MHz reference frequency (fREF) is applied to pin 5 of IC4 (CXD1225M) and is divided internally by 500 (2000 in FM mode), to produce a 20-kHz (5-kHz in FM mode) comparison frequency. The output from VCO2 is applied to pin 11 of IC4, and is divided internally by 3211 (12844 in FM mode). It is then compared with the 20-kHz (5-kHz in FM mode) reference signal by the phase comparator to lock the VCO2 frequency. Divide ratio data is supplied by the digital unit.

The output is amplified to about 5dBm by amplifier Q17 and passes through a low-pass filter. The imped ance is converted and the signal is output.

3) LO1 PLL loop

Four VCOs, Q1 to Q4 (2SK210 x 4), generate 73.08- to 103.05-MHz signals. The reference signal of 10MHz is applied to pin 5 of IC3 (CXD1225M) and is divided by 20 internally to produce a 500-kHz comparison frequency. The output signal passes through amplifier Q12 and a band-pass filter, and is divided into two signals. One signal passes through the buffer and low-pass filter of Q14 (2SC2996) and is output to the RF unit.

The other signal is applied to pin 5 of mixer IC6 (SN76514N). The DLO1 signal of 4.45 to 4.95MHz is input to pin 5 of mixer IC from the carrier unit, and a 60-MHz signal (3 times the 20-MHz reference signal) is input to pin 1. The signal of 55.05 to 55.55MHz signal from mixer IC1 is applied to pin 11 of mixer IC6, and becomes a signal of 18.03 to 48.0MHz. The signal is output from pin 13, passes through the high-pass and low-pass filters, amplifiers Q16 (2SC2714) and Q15 (2SC2712), and is applied to pin 11 of IC3 (CXD1225M).

This signal is divided by N1 internally, compared with a 500-kHz signal by the phase comparator, and the mixer output frequency is locked in 500-kHz steps. Divide ratio N1 is sent from the digital unit as data (76 to 136) that covers 30kHz to 30MHz in 500-kHz steps. One of the four VCOs is selected according to the VCO switching data from the digital unit.

DLO1 sweeps 4.45 to 4.95MHz in 10-Hz or 1-Hz steps. The LO1 output covers 73.08 to 103.05MHz in 10-Hz or 1-Hz steps, and is output to the RF unit.

4) PLL data

The TS-850 has two PLLs as shown below, to which the main microprocessor sends PLL data based on the frequency indicated for each of the PLLs..

- VFO PLL
- Local oscillator PLL for frequency conversion

The VCOs are selected depending upon conditions:

- Main encoder changes → VCO1
- Mode changes → VCO2

When each PLL IC outputs an unlock signal and one of the PLLs is unlocked, the display is changed to "....." (decimal points only) to indicate that a PLL is unlocked.

Unlocking of each PLL can be confirmed by the fact that the status is output to the A0 terminal of pin 8 of the PLL IC (CXD1225M) as UL data.

Loop	VCO No.	IC No.	Comparison freq'/ Divide ratio	Variable divide ratio	Frequency (MHz)
LO1	VCO1	IC3	500k/20	36~96	73.08~103.0
LO2	VCO2	IC4	20k/500 5k/2000 (FM)	3211 12844 (FM)	64.22

CAR Unit

The TS-850 CAR unit has four newly developed DDS ICs, and generates small PLL steps (DLO1) that cover 10kHz to 30MHz in 1-Hz steps, the third local oscillator (LO3), CAR (CAR, MCAR), sidetone (STON), and subcarrier signals. Kenwood's original DDS IC frequency modulation function is provided for FSK and subtone modulation.

1) Reference signal

The 20-MHz reference signal from the PLL unit is amplified by Q3, buffered by CMOS inverter IC9, and supplied to the DDS ICs (IC1 to IC4) and IC5. This signal is halved by IC1 to IC4 to produce a DDS reference signal. It is divided by 5 by IC5, and a 4-MHz signal is supplied to the mixer that converts the IC1 output to DLO1.

2) DLO1 generation

Digital signals from 0.95 to 0.45MHz are generated by IC1, converted to analog signals by the digital-to-analog (D/A) converter consisting of CP1, CP2, and Q1, passed through a low-pass filter, and are then applied to mixer IC6. Here they are mixed with a 4-MHz signal from IC5. The resulting signal is filtered by a combination of high-pass and low-pass filters to produce a signal in the range of 4.95 to 4.45MHz. This signal is output from buffer Q2 to the PLL unit as DLO1.

CIRCUIT DESCRIPTION

3) LO3 generation

IC2 generates a digital signal with a basic frequency of about 1.625MHz. The signal is converted to an analog signal by the D/A converter consisting of CP3, CP4, and Q4, and chopped by a circuit consisting of Q5, Q6, and Q7 to extract the first harmonic component of about 8.375MHz. Undesired components of this signal are removed by ceramic filters CF1 and CF2. The resulting signal is amplified by Q8 and Q9, and output as the LO3 signal. During FM transmission, digital data from IC3 is input to the modulator to perform sub-tone modulation.

4) CAR generation

A digital signal of about 455kHz is generated by IC4, converted to an analog signal by the D/A converter consisting of CP7, CP8, and Q17, buffered by Q18, passed through a low-pass filter, and output as the CAR signal.

In the FSK mode, FSK modulation is performed directly by IC4 using the RTK signal supplied via digital transistor Q19 for level conversion.

5) MCAR generation

When transmitting in the SSB and FSK modes, IC3 generates a digital signal with a basic frequency of about 1.17MHz. The signal is converted to an analog signal by the D/A converter consisting of CP3, CP4, and Q4, and chopped by a circuit consisting of Q11, Q12, and Q13 to extract the first harmonic component of about 8.83MHz. Undesired components are removed by ceramic filters CF3 and CF4, and the resulting signal is amplified by Q14 and Q15, and output as the MCAR signal.

6) STON generation

In the CW mode, a digital signal of the CW pitch is generated by IC3, converted to an analog signal, passed through buffer Q16 and CR filter, and output as the STON signal.

7) Subtone generation

When transmitting in the FM mode, IC3 generates a digital subtone frequency, and directly outputs it to IC2 without converting it to an analog signal.

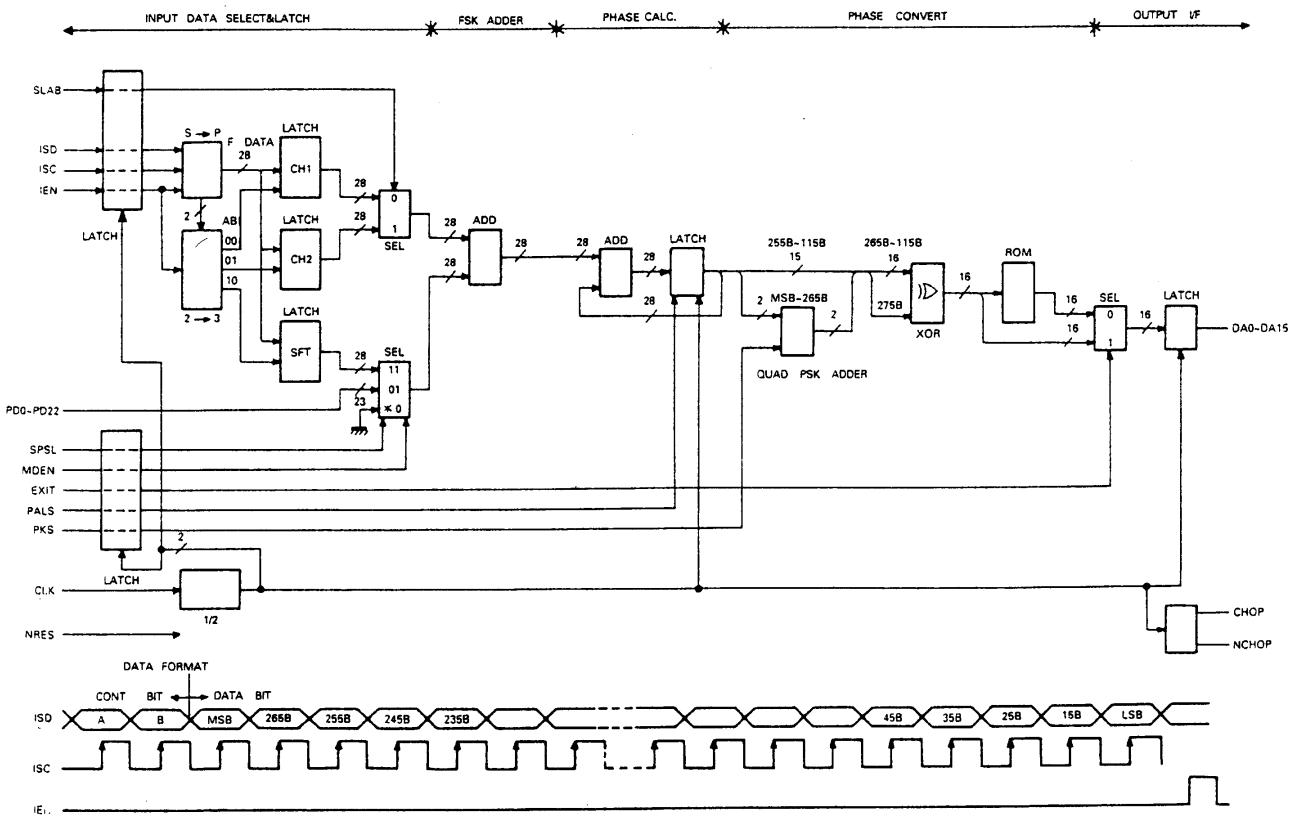


Fig. 4 DDS IC : YM6631 block diagram and data format

CIRCUIT DESCRIPTION

8) DDS

The DDS IC has been developed with standard cells to implement a high-speed circuit and large-capacity ROM at a low cost.

- **IC configuration**

There are two 28-bit registers for programming frequency data, one 28-bit frequency shift register for addition to the frequency registers, a 23-bit parallel signal input section for frequency modulation with parallel signals, and a data entry and selection section.

There is a frequency-modulation section consisting of 28-bit adders for adding frequency data and frequency modulation data; a phase data operation section that adds data from the frequency modulation section and 28-bit phase data register; and a SIN-ROM that converts phase data to sine signals.

- **Frequency/shift data setting**

30 bits (2 bits that specify the destination for which data is set and 28 bits for frequency data) are set in the three internal registers using serial signals synchronized with the internal clock.

- **Frequency register selection**

The data set in the two frequency registers is selected by the SLAB input of the DDS IC. This pin handles the ABSL signal for IC1 and IC3, and the CASL signal for IC2 and IC4. This function eliminates the need for the TS-850 to set frequency data for each transmission/reception with the microprocessor.

- **Frequency data selection**

The SPSL input of the DDS IC selects whether to use the data in the internal frequency shift register or the data from the parallel input as frequency modulation data.

- **Frequency modulation**

The MDEN input of the DDS IC enables or disables frequency modulation. When frequency modulation is enabled, frequency data is added, and the result is input to the phase data operation section.

- **Phase data operation**

The desired frequency phase data is output by collecting 28-bit frequency data in the 28-bit phase accumulator.

$$Fout = Fs/2^{28} \cdot Dsum$$

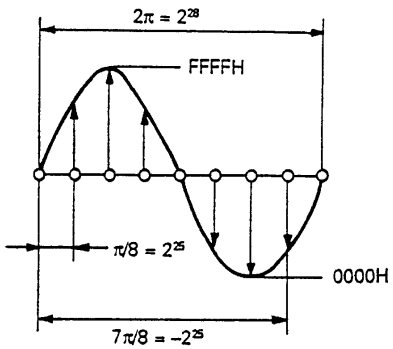
Fs : DDS IC input frequency/2
Dsum: Frequency data + Frequency modulation data

If 2^{25} is set for Dsum when 1/8 Fs is output, the phase data must be increased by1/8.

A 28-bit absolute value operation has been used so far, but a 28-bit signed operation can also be used, assuming that the MSB is a sign. If complementary data of 8000000 to FFFFFFFF (hex) is set, the phase moves in the negative direction for the positive data.

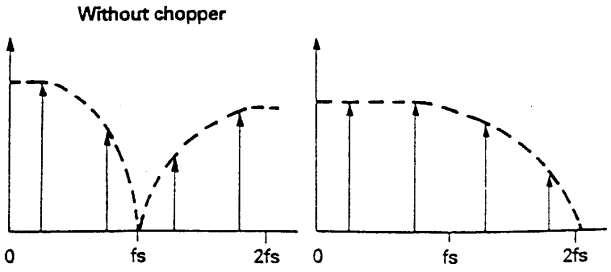
- **SIN ROM**

Phase data from the phase data operation section is converted to sine data of 0000 to FFFF (hex) in the 16-bit offset binary format.



9) Chopper

When the output from the DDS IC is converted to an analog signal by the D/A converter with a ladder resistor network, the possible output frequency range is 0 to Fs/5. To obtain an output of 8.83/8.375MHz, 1.17/1.625MHz is produced and then converted to 8.83/8.375MHz by a mixer. When the DDS output spectrum is seen when Fs is 10MHz, the basic frequency of 1.17/1.625MHz and a harmonic component of 8.83/8.375MHz can be recognized. The level of this signal component is lower than the basic signal level because of the aperture effect, and the C/N ratio is less than ideal. The D/A output is extracted as a series of thin rectangular pulses by the chopper that are used to increase the level to that of the basic signal level, and thus obtain an output with a good C/N ratio. Use of the chopper eliminates the need for a filter in the mixer input.



CIRCUIT DESCRIPTION

Receiver Circuit Description

The basic configuration of the receiver circuit is that of a triple-conversion superheterodyne. Fig. 5 shows the frequency configuration.

The incoming signal from the antenna is switched to the receiver by the antenna switching relay on filter unit (B/3). The signal passes through an image filter, and is applied to the CN1 (RAT) terminal of the RF unit via a coaxial cable. The signal is amplified by the first and second RF amplifiers and is then applied to the 1st RX mixer. Here the signal is converted into the 1st RF signal of 73.05MHz. The signal is then applied to a 73.05MHz MCF (Monolythic Crystal Filter) to remove unwanted components, that result from the mixing process, from the incoming signal. The 1st RF signal is then applied to the 2nd RX mixer in order to obtain the 2nd RF frequency of 8.83MHz. The resulting signal is then filtered to remove the unwanted components that result from the mixing action. Signals are transferred to and from the IF unit at 8.83MHz. The signal is converted to 455kHz by a third RX mixer in the IF unit, and processed to produce an audio signal.

The differences in operations between the TS-850 and some of Kenwood's previous models are listed below.

RF ATT: The 10-dB step has been changed to provide 6-dB steps.

RF band-pass filter: Two low-pass filters and 10 band-pass filters are used for 100kHz to 30MHz. For frequencies beyond the BC band, interference by high-output AM stations is minimized by passing the signals through a high-pass filter of fc = 1.6MHz. The undesired signals in the 7-, 14-, and 21-MHz antenna bands are removed by a special adjustable narrow-band band-pass filter. The TS-850 also uses these band-pass filters in transmit mode to transmit radio signals with few spurious signals.

RF amplifier: If AIP is off, an RF amplifier is inserted before the first mixer. If the frequency is 22MHz or less, the NFB amplifier using J-FETs (Q2, Q3, 2SK125-5) for good large input characteristics is selected automatically. If the frequency is higher than 22MHz, the amplifier using a MOSFET (Q1, 3SK131) for good sensitivity is selected automatically.

RF gain: The RF gain does not work in FM mode to prevent squelch malfunctions.

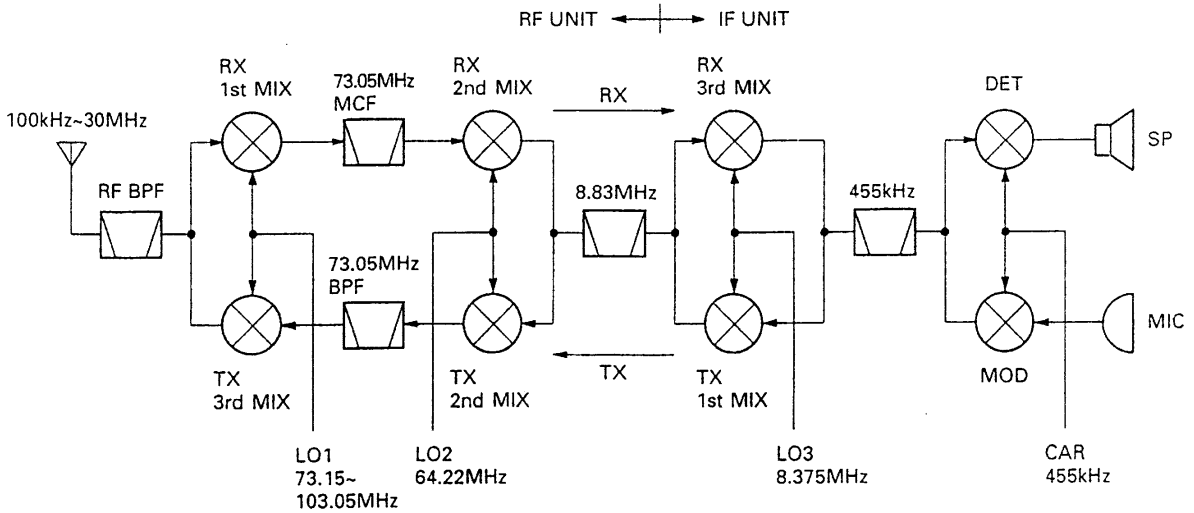


Fig. 5 Frequency configuration

CIRCUIT DESCRIPTION

1) RF band-pass filter switching signal decoding

There are 12 bands to be switched, but only 10 outputs from IC1. The two extra bands are generated by a logic circuit consisting of IC2, Q48, Q6, and Q7.

IC1 input logic				Decoder output	
15 pin	14 pin	13 pin	12 pin	Pin that goes low when active	Band-pass filter
L	H	L	L	3	0.1~0.5MHz
H	L	L	L	2	0.5~1.62MHz 0.5~1.705MHz (K type)
L	L	H	L	5	1.62~2.5MHz
L	L	L	H	10	2.5~4MHz
L	H	L	H	Q6	4~7MHz
L	L	L	L	1	7~7.5MHz
H	H	H	L	9	7.5~10.5MHz
H	H	L	H	Q7	10.5~14MHz
H	H	L	L	4	14~14.5MHz
H	L	L	H	11	14.5~21MHz
L	H	H	L	7	21~22MHz
H	L	H	L	6	22~30MHz

2) RF amplifier switching and AIP switching

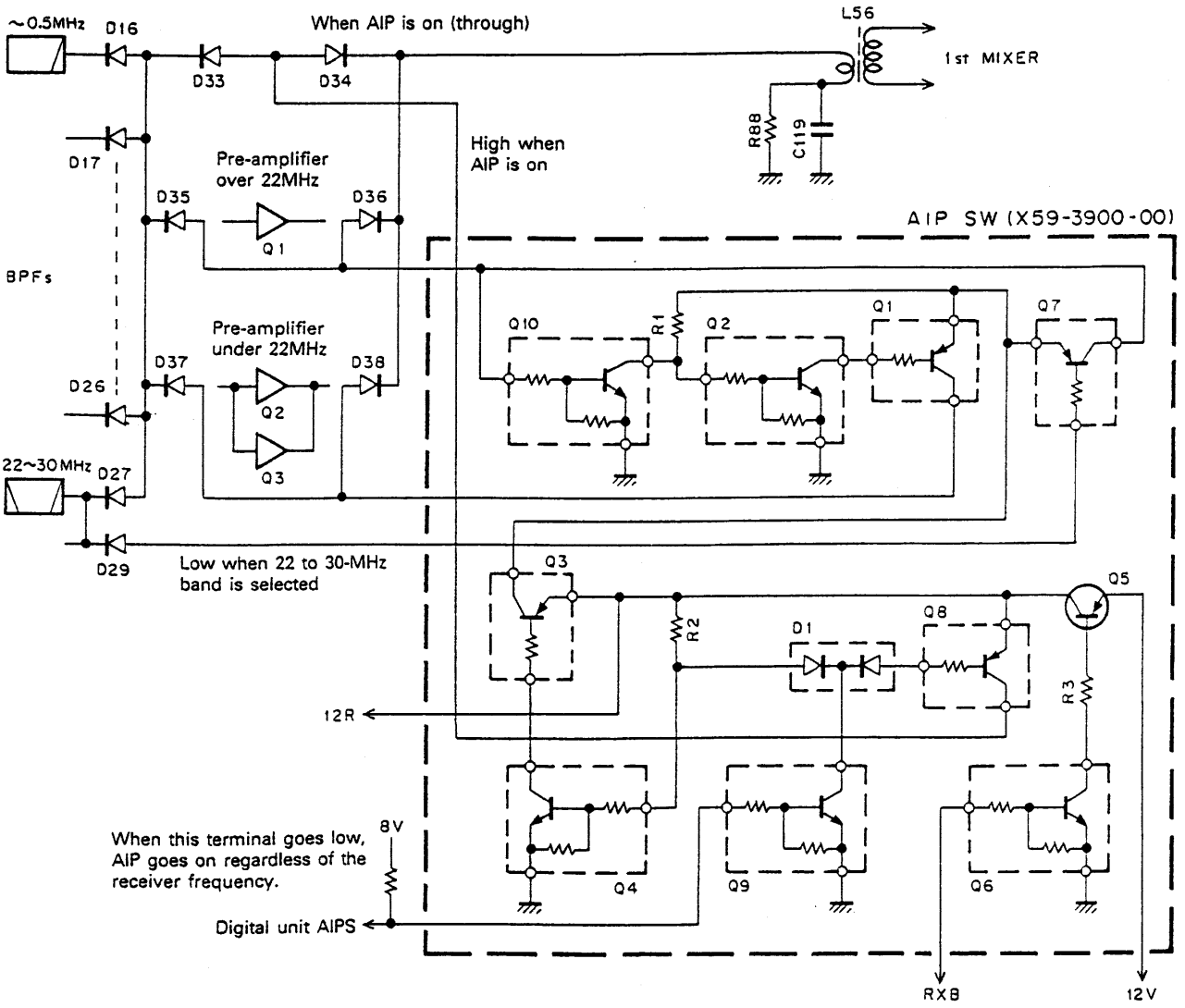


Fig. 6 RF amplifier switching and AIP switching

CIRCUIT DESCRIPTION

3) Noise blanker

The circuit up to the detection stage is the same as previous versions of this circuit. When the NB1 switch is on, the noise pulse passes through Q605, Q607, and D604, and drives the NB gate. Since Q606 power is off, the pulse signal is not transmitted any farther, and NB2 does not operate. When the NB2 switch is on, the noise pulse passes through Q606, Q608, and D604.

Previous versions of NB2 had a problem that occured when the blanking time increased, the signal was blanked and the desired signal was not obtained if there was a noise with a short period, such as ignition noise. This meant that the blanking time had to be about 5ms. Considering the fact that the period of woodpecker noise is generally 100 nsec, the TS-850 has a pulse period identification circuit that passes only pulses with a period of 100ms ± about 30ms to minimize the possibility of malfunction due to noise even if the blanking time is increased.

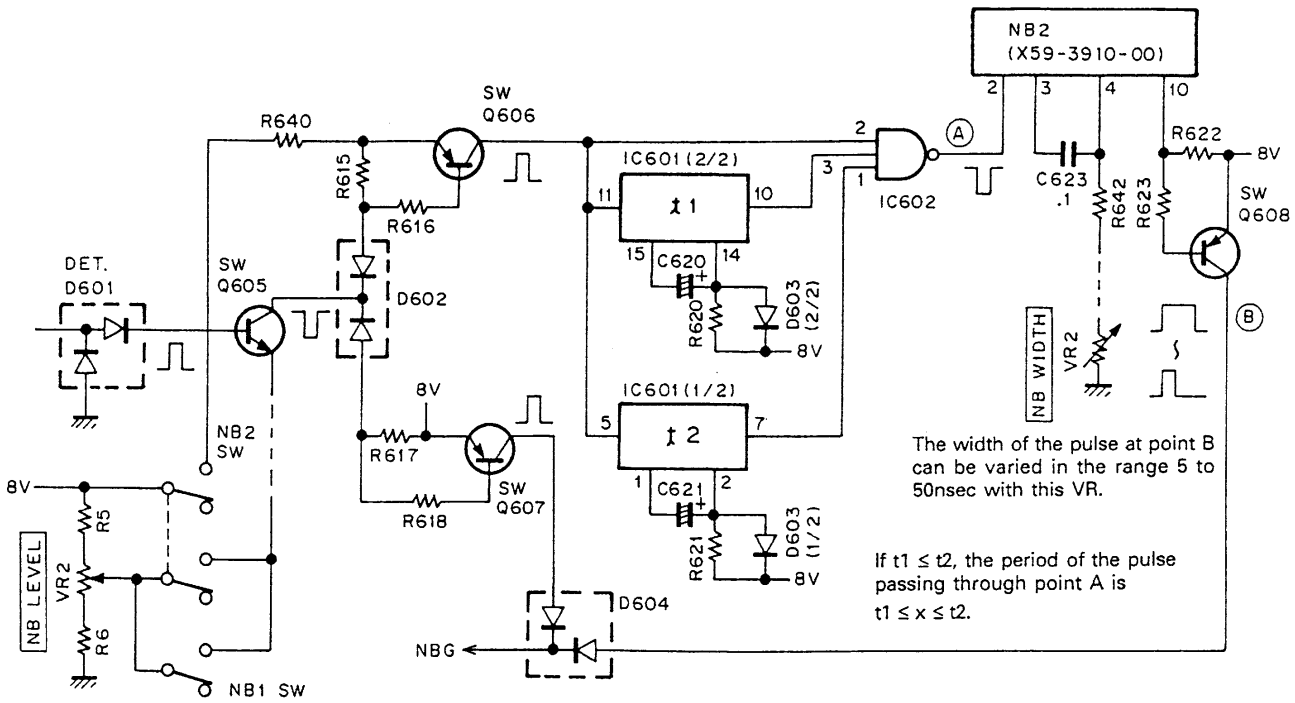


Fig. 7 Noise blanker circuit

CIRCUIT DESCRIPTION

4) IF filter selection

Two optional 8.83-MHz filters and one 455-kHz filter can be installed.

Initial condition

Display	8.83MHz	Display	455kHz
No display	Through (LC filter)	12kHz	L72-0315-05
6kHz	L71-0266-05	6kHz	L72-0319-05
2.7kHz	L71-0222-05	2.7kHz	L72-0333-05
500Hz*	Option (not installed)	500Hz*	Option (not installed)
270Hz*	Option (not installed)		

Frequencies marked * are not displayed by operating the filter changeover switch. They can be displayed by setting the corresponding bit of S501 in the RF unit (X44-3120-00 C/4) on when an optional filter is installed.

Optional filter types

8.83MHz		455kHz	
500Hz	YK-88C-1	500Hz	YG-455C-1
270Hz	YK-88CN-1		

Filters with bandwidths other than the ones described above can be installed. If this is done, the bandwidth displayed on the main display would not correspond with the actual bandwidth.

Item	Rating
Nominal center frequency	73.05MHz
Pass bandwidth	±7.5kHz or more at 3dB
Attenuation bandwidth	±30kHz or less at 40dB
Ripple	1.0dB or less
Insertion loss	3.0dB or less
Guaranteed attenuation	70dB or more at fo + (500 to 1000) kHz) 70dB or more at fo – (200 to 1000) kHz
Center frequency deviation	Within ±1.5kHz at 3dB
Input and output impedance	2kΩ ± 10%

MCF (L71-0401-05) (RF unit XF1)

Item	Rating
Nominal center frequency	8830kHz
Center frequency deviation	Within ±150Hz at 6dB
Passband width	±1.3kHz or more at 6dB
Attenuation bandwidth	±1.7kHz or less at 20dB ±2.5kHz or less at 60dB ±3.4kHz or less at 80dB
Ripple	2dB or less
Insertion loss	6dB or less
Guaranteed attenuation	80dB or more in the range ±3.4kHz to ±1MHz
Input and output impedance	600Ω / 15pF

MCF (L71-0222-05) (RF unit XF2)

Item	Rating
Nominal center frequency (fo)	8830kHz
Pass bandwidth	fo ± 3.0kHz or more at 6dB
Attenuation bandwidth	fo ± 16.0kHz or less at 60dB fo ± 13.0kHz or less at 50dB
Guaranteed attenuation	70dB or more within fo ± 1MHz
Ripple	Within 1.0dB
Insertion loss	Within 1.5dB
Input and output impedance	1850Ω / 2pF

MCF (L71-0266-05) (RF unit XF3)

Item	Rating
Nominal center frequency	455 ± 0.20kHz
6dB bandwidth	2.9 to 3.2kHz
60dB bandwidth	4.7kHz or less
Guarateed attenuation	60dB or more at 0.1 to 1MHz
Spurious	40dB or more at 600 to 700kHz
Ripple (in 6dB band)	2dB or less
Insertion loss	6dB or less
Guaranteed attenuation	60dB or more within ±40kHz
Input and output impedance	2kΩ

Ceramic filter (L72-0333-05) (IF unit CF1)

Item	Rating
Nominal center frequency	455kHz
6dB bandwidth	±6kHz or more (at 455kHz)
50dB bandwidth	±12.5kHz or less (at 455kHz)
Ripple (within 455 ± 4kHz)	3dB or less
Insertion loss	6dB or less
Guaranteed attenuation (within 455 ± 100kHz)	35dB or more
Input and output impedance	2.0kΩ

Ceramic filter (L72-0315-05) (IF unit CF2)

Item	Rating
Nominal center frequency	455kHz
6dB bandwidth	±3kHz or more (at 455kHz)
50dB bandwidth	±9kHz or less (at 455kHz)
Ripple (within 455 ± 2kHz)	2dB or less
Insertion loss	6dB or less
Guaranteed attenuation (within 455 ± 100kHz)	60dB or more
Input and output impedance	2.0kΩ

Ceramic filter (L72-0319-05) (IF unit CF3)

CIRCUIT DESCRIPTION

Transmitter Circuit

The audio signal from the microphone enters CN22 of the IF unit. The signal is split and directed to input/output connector CN21 of the optional DRU-2 and the microphone amplifier module (X59-3850-00). The microphone amplifier module contains a microphone amplifier with a gain of about 20dB and a mixer for data entry. The audio signal is amplified by the microphone amplifier, passes through the mixer, and is output from the microphone amplifier module.

The signal output from the microphone amplifier module is split and directed to the microphone amplifier output for the optional DSP-100, the FM microphone amplifier, and the SSB, AM microphone gain potentiometer. SSB is mainly explained below. The FM system will be described later.

The signal that is controlled by the microphone gain potentiometer (processor potentiometer when a speech processor is used) on the front panel, enters CN of the IF unit. The microphone gain potentiometer or processor potentiometer output is switched by the microphone switch module (X59-3840-00). The signal from the microphone switch module is amplified by Q26 and modulated to 455-kHz DSB by the balanced modulator (IC3). The carrier (CAR) is generated by the DDS in the carrier unit (X50-3140-00) (about 0dBm), and enters CN9 of the IF unit. LO4 is split and directed to the buffer amplifier (Q25) for the receive and transmit carriers. LO4 from the buffer amplifier passes through the pin diode (D28) for carrier level adjustment, and enters the balanced modulator (IC3). This diode is completely on in SSB.

The DSB signal passes through ceramic filter CF1 (2.7-kHz band) and is converted into an SSB signal. The signal passes through the buffer amplifier (Q9), and is mixed with LO3 (8.375MHz) generated by the DDS in the carrier unit to produce 8.83MHz. The 8.83-MHz SSB signal enters CN19 of the RF unit from CN6 of the IF unit.

The signal entering the RF unit passes through ceramic filter CF1 (2.7-kHz band),amplifier (Q20) to which ALC is applied, and pin diode (Q89) that controls the gain when the power is controlled, and is converted to 73.05MHz by the second mixer (Q23, Q24). The signal passes through a three stage LC filte, and is converted to the desired frequency by the final mixer. The SSB signal converted to the desired frequency passes through the receive band-pass filter, is amplified by RF drive amplifier (Q5), and output to the final unit from CN2.

The signal is amplified to about 100W by the final unit. Harmonic components are attenuated by the filter unit, and the signal is output from the antenna connector.

In AM a DC bias is applied to the balanced modulator (IC3) of the IF unit in order to unbalance it and pass the signal. The carrier level is controlled by setting the current flowing to the pin diode for carrier level adjustment to an appropriate level with the CAR potentiometer on the front panel. For FM, the output from the microphone amplifier module enters CN603 of the RF unit (B/4) from CN23 of the IF unit, passes through the FM microphone amplifier module (X59-3000-03) of the pre-emphasis and IDC circuit, is output from CN603, enters CN8 of the PLL unit, and LO2 (64.22MHz) is modulated.

The carrier for CW, FM, and FSK is adjusted to an appropriate level by changing the current thru pin diode (D28) in the IF unit with the carrier potentiometer. The carrier passes through W1 on the bypass line of the 455-kHz ceramic filter, enters the first mixer, is converted to 8.83MHz, and enters the RF unit. The signal passes through the same route as for SSB and is transmitted from the antenna. CW keying is performed by the ALC voltage and the first and second gates of the second mixer.

CIRCUIT DESCRIPTION

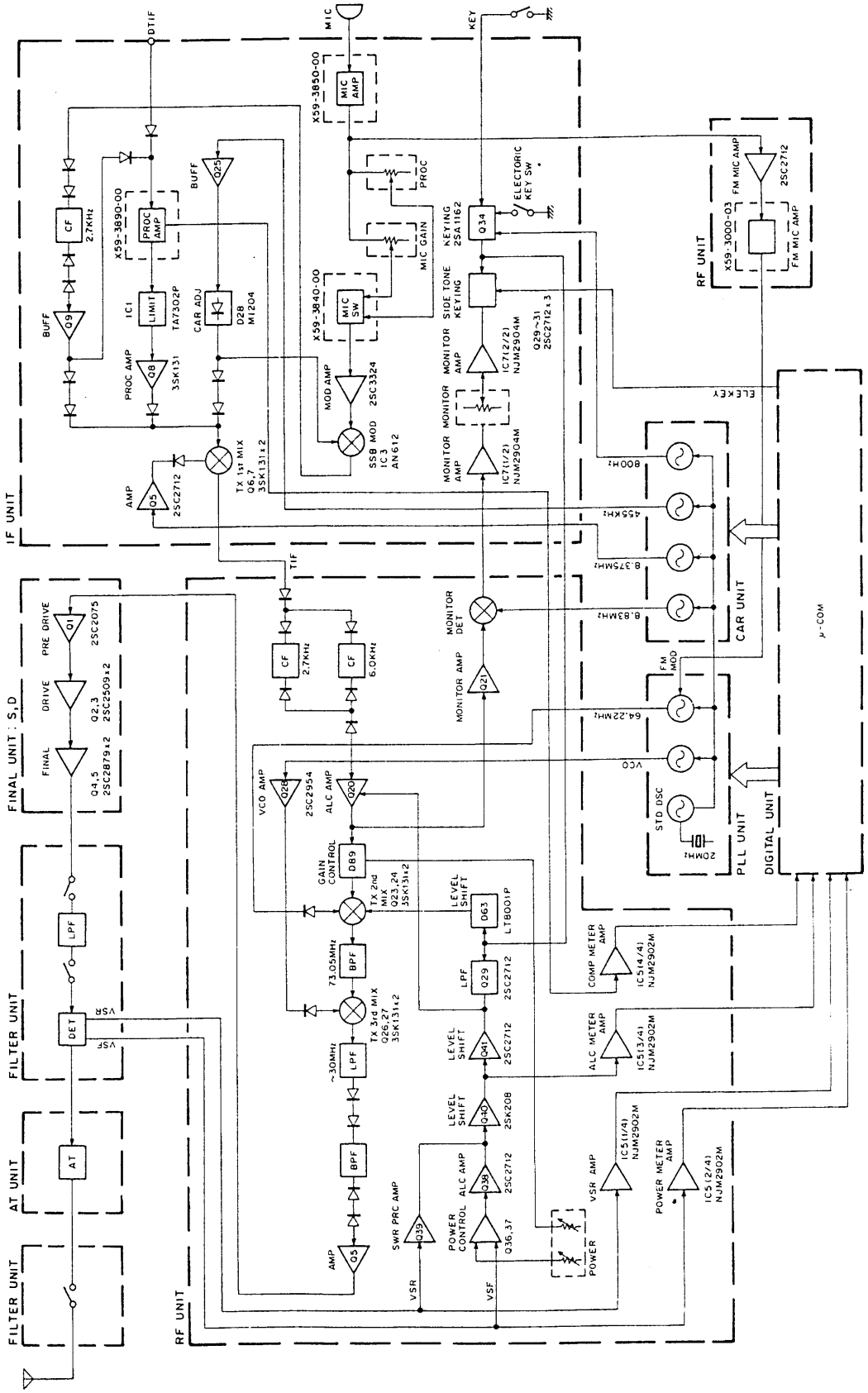


Fig. 8 Transmitter circuit block diagram

CIRCUIT DESCRIPTION

1) Power control and power settings

The TS-850 power is controlled in almost the same way as the TS-950. The forward wave voltage detected by the filter unit enters the RF unit, is set to an appropriate level by resistor (VR7), and enters differential amplifier (Q36, Q37). The gain of this differential amplifier is changed by changing the base voltage of Q37. If the power is relatively low, such as in the S-type minimum power condition or AT-TUNE condition, the base voltage of Q37 is decreased, and the gain of the differential amplifier is increased. When the gain of the differential amplifier is increased, the apparent forward wave voltage increases, and the ALC circuit operates with less power, and the maximum power is reduced.

If the drive level is not decreased as the power is decreased, over-drive occurs. To prevent this, the gain of the amplifier of the signal system in the ALC loop is decreased. This changes the ALC level and changes the current through pin diode (D89) of the RF unit (by means of VR11 B/2 of the switch unit [F/6]) to set the drive level to an appropriate level. The difference between the TS-850 and TS-950 is that the TS-850 has a ceramic trimmer (TC1) connected to the pin diode in parallel to adjust and correct the minimum drive level.

In AT-TUNE, Q31 is turned on and Q34 is turned off by the ATPD signal from the microprocessor to disconnect VR11. Q52 is turned on to connect R297 to the base of Q37 to keep the power at 10 W regardless of the power control potentiometer position. Q30 is turned on and Q32 is turned off, and VR4 (TYP) for 50-W adjustment is also disconnected. The resistance of R297 determines the power for AT-TUNE.

The TUNE mode is similar: when the TPD signal goes low, Q46, Q30, Q31, and Q35 are turned on, the power control potentiometer (VR11 A/2) and 50-W setting potentiometer (VR4, TYP) are disconnected, and potentiometer (VR6, TUNE) for the TUNE mode is connected to the base of Q37.

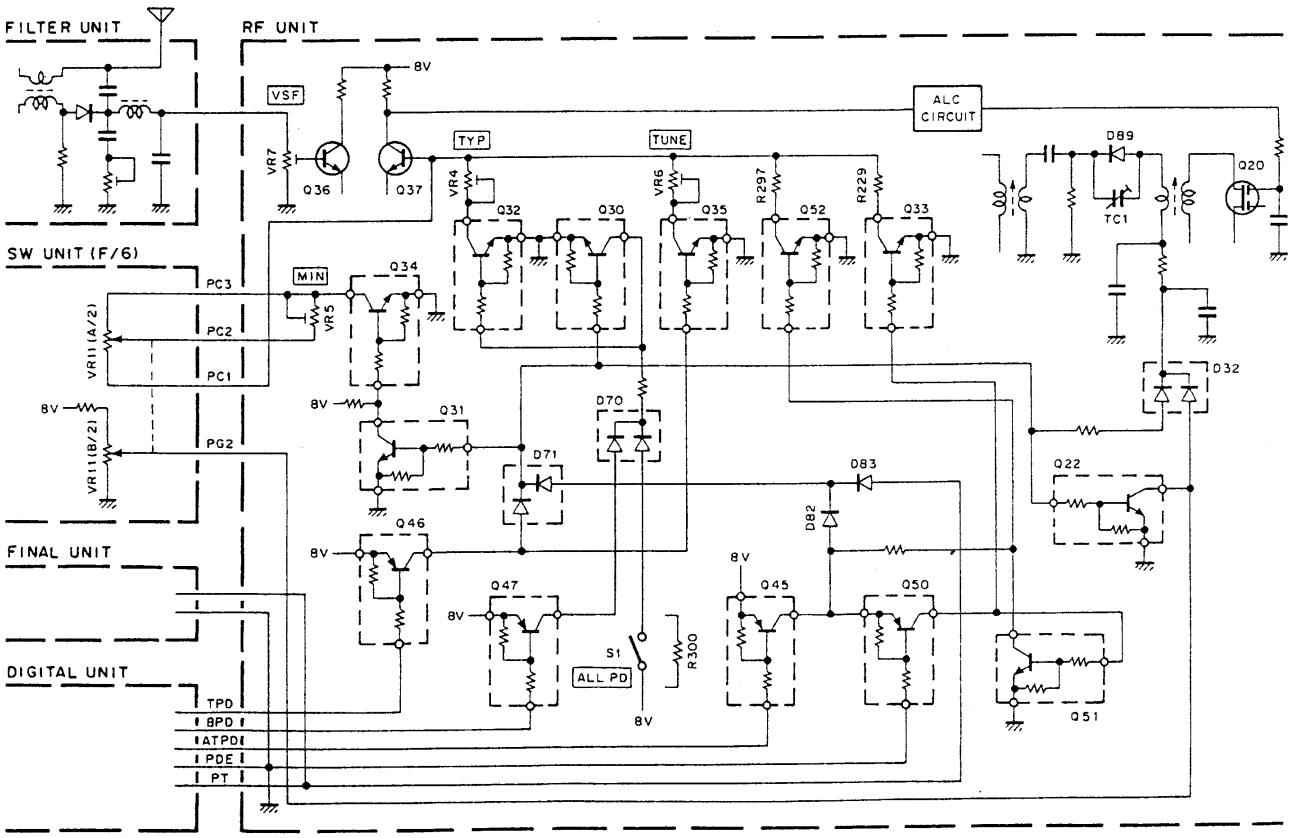


Fig. 9 Power control and power setting

CIRCUIT DESCRIPTION

2) Voice memory operation

If the optional DRU-2 is installed, the voice memory can be used.

Logic for VOA and VOB

	Recording	Monitor	Transmission
VOA	L	H	H
VOB	H	L	H

1) During recording
Signals from the microphone are sent to the VI terminal of the DRU-2 and are stored into memory on the DRU-2.

2) During recall
Signals from the DRU-2 are sent to IC7 A/2 of the IF unit, and amplified to drive the speaker. The potentiometer can be varied by the monitor VR on the panel. It is independent of the AF VR setting.

3) During transmission
Signals from the DRU-2 are output from VI and sent to the microphone amplifier.

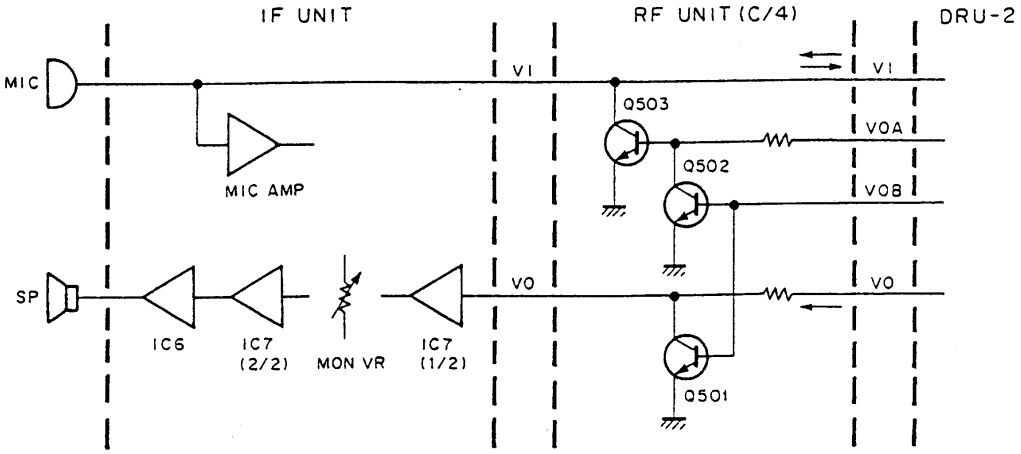


Fig. 10 Voice memory operation

Filter Unit

1) Transmit low-pass filter, AT band data

Transmit band data (TB0 to TB3) from the digital unit passes through the RF unit and digital unit (D/4), and is directed to the filter unit.

The switching signal split and decoded by the filter unit selects the transmit low-pass filter in the filter unit, and the AT band of the AT unit.

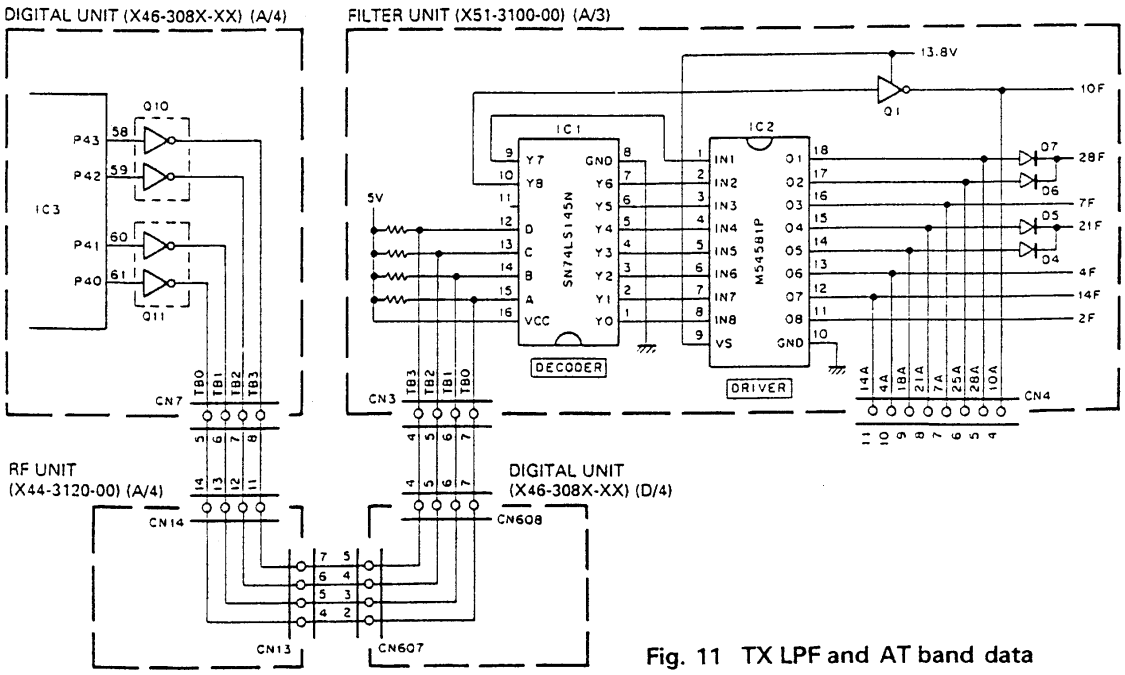


Fig. 11 TX LPF and AT band data

CIRCUIT DESCRIPTION

AT Unit

1) Auto antenna tuner

When the AUTO/THRU switch is set to AUTO, the signal is convertedby the digital unit, ATA goes low, the AUTO/THRU switching relay K1 closes, and the AT is inserted to prepare for tuning. If variable capacitors VC1 and VC2 are not at their preset positions, they are set to the preset positions. AT TUNE operation and-transmission do not start until the preset has been completed.

When AT TUNE is turned on, ATS goes high, the mode is switched to CW, and the transmitter output becomes about 10W. If the VSWR is less than 1.2, tuning is regarded as completed, and the AT TUNE operation stops.

If the VSWR is greater than 1.2, the duty cycle of the motor control pulse (described later) is varied according to the VSWR.

The motor speed is determined by the microprocessor, and the direction is determined by the phase comparator (IC1) and amplitude comparator (IC6) if the APRE is low, and by the microprocessor if the APRE is high.

- **Auto tuning mode**

The transmitter power from the final unit passes, via the filter unit, through current/voltage detection transformers L1 and L2, which have toroidal cores. The current and voltage components detected here are rectified by a waveform rectification circuit consisting of D4, Q1, D7, and Q2, and are then phase-compared by IC1 (SN74S74N). The output signals ($\overline{Q}$ and Q) from pins 8 and 9 of IC1 are passed through the switch by IC2 (TC4066BP), and are applied to the motor drive IC (IC4). Variable capacitor VC1 is turned by motor M1 so that the phase difference of the voltage and current components decreases.

The voltage and current components detected by L1 and L2 are rectified by germanium diodes (1N60) D1 and D2, and are applied to voltage comparison circuit IC6 (NJM2903S) as the amplitude component of the signal. The comparator output is passed through the switch by IC3 (TC4066BP). Motor M2 is driven by another motor drive IC, IC5 (BA6109U2), which turns variable capacitor VC2 in the direction that decreases the amplitude difference of the voltage and current components.

Therefore, variable capacitor VC1 adjusts the capacitance of the circuit so that the current and voltage phases match, and variable capacitor VC2 adjusts the resistance of the circuit so that the current and voltage amplitude difference decreases. If the phases match and the amplitude difference is zero, the SWR is 1 : 1.

The speed of motors M1 and M2 is determined by the duty cycle of the pulse input to control input pin 8 of IC4 and IC5. It is controlled according to the VSWR calculated by the CPU in the digital unit and the speed corresponding to preset or manual tuning.

Pulse signal SPED output from the digital unit passes through Q5 (DTC114EK), and is amplified by Q4 (2SA1204) to produce a control pulse input to IC4 and IC5.

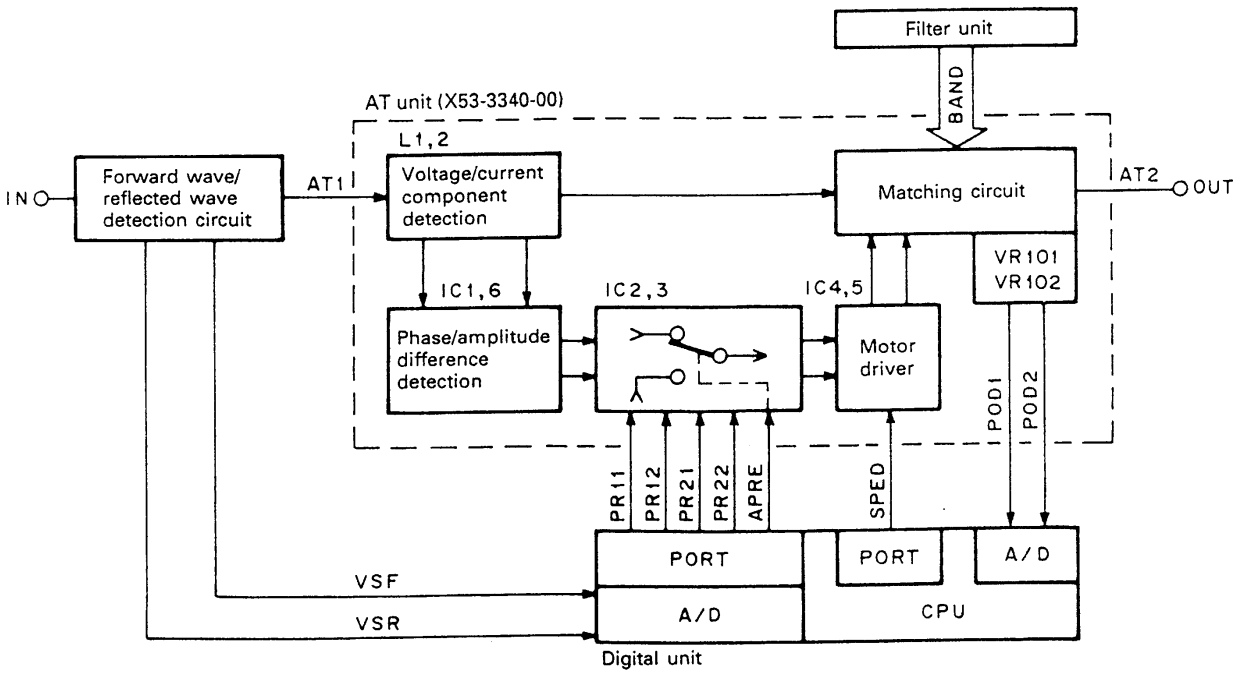


Fig. 12 Block diagram of auto antenna tuner

CIRCUIT DESCRIPTION

When the SWR is 3 : 1 or more, the motor runs at high speed since the duty cycle of the motor drive voltage pulse is 100%. When the SWR is 2 : 1, the duty cycle becomes about 50%, and the motor runs at low speed.

The matching circuit used in the tuner is a T type. The tap position from 1.8 to 30MHz is controlled by seven relays, K101 to K103, and K105 to K108.

Position detection potentiometers VR101 and VR102 are linked to the spindles of variable capacitors VC1 and VC2 with a gear ratio of 1 : 1. Voltages of 0 to 5V (POD1 and POD2) are generated according to the positions of the variable capacitors. This position data is supplied to the CPU through the A/D converter by the digital unit, and is used as the reference voltage in the feedback control system, which is used for preset tuning and manual tuning. The same signal is also used for preset data and to signal the completion of tuning.

The potentiometers used here are not ones that rotate through 360 degrees. Since the rotation angle of each potentiometer is limited, the rotation range is from the minimum capacitance to the maximum capacitance, plus a little extra for headroom.

Through this control, like preset tuning, which will be described later, POD1 and POD2 are monitored by the microprocessor. If the lower limit voltage of 0.6V or the upper limit voltage of 4.2V is reached, the microprocessor detects that a variable capacitor is close to one of its limits. To return the voltage to the opposite side, APRE is switched high. For VC1, if the voltage is close to the lower limit with respect to PRE1, the voltage near the upper limit is output. If the voltage is close to the upper limit with respect to PRE1, the voltage near the lower limit is output.

If the variable capacitor voltage exceeds the specified limit, the variable capacitor is returned to the opposite limit. The other variable capacitor remains in the same position.

The direction of the motor is determined by the CPU unless auto tuning is performed with high APRE. The logic of PR11 to PR22 is the same as the logic of IC4 and IC5 (BA6109U2). The signal output from the digital unit passes through IC2 and IC3 (TC4066BP), and is input to IC4 and IC5 (BA6109U2).

		PR11	PR12	PR21	PR22
Motor 1	Normal rotation	H	L	-	-
	Reverse rotation	L	H	-	-
Motor 2	Normal rotation	-	-	H	L
	Reverse rotation	-	-	L	H

The motor stops in other cases.

- **Manual tuning**

Hold down the USB/LSB key and switch the power on. Select menu number 20 with the encoder, turn the display off with the band down key, and press the CLR key to return to the normal mode. Manual tuning is now possible.

The main encoder is used to control VC1, and the sub-encoder is used to control VC2. The capacitance of each variable capacitor changes from the maximum to the minimum when the encoder is turned about eight turns.

- **Preset tuning**

When auto or manual tuning stops, the position of the variable capacitor is stored in memory by the microprocessor as preset data for that band.

When the band is changed after tuning is performed in another band, APRE goes high, the motor is controlled by the microprocessor, and preset tuning is performed. During preset tuning, auto tuning or signal transmission is inhibited even if the AT TUNE switch is pressed or transmission becomes ready.

The initial preset data when the microprocessor is reset includes standard data for a 50 ohm load on each band.

CIRCUIT DESCRIPTION

Standby Control Timing

Standby control and timing are handled by the IF unit (X48-3080-00). The following control signals are used:

SS : Standby switch. Active low.
KEY : Keying signal from the keyer. Active low.
TXI : Transmission inhibit signal from the microprocessor. Low when transmission is inhibited.
PKS : Standby signal from the data communication terminal. Active Low.

The control output signals are as follows:

TXB : 8 V during transmission
RXB : 8 V during reception. Reversal of TXB.
CKY : Keying output signal. Active High.
RBC : Receive control signal. Active Low.

1) Manual standby (except CW)

- **RX → TX**

If pin 9 (TXI) of the BK-SW module (X59-3880-00) is high when the standby switch is pressed and the SS line is grounded, Q2 in the module is turned on, and the base of Q49 is grounded via pin 10.

The collector of Q49 goes high, the signal enters pin 10 of the BK-IN module (X59-3870-00), passes through D1 in the module, enters pin 2 of the TRX module from pin 2 via R132, passes through the internal switch circuit, and TXB is output from pin 5. When TXB is high, RXB is low.

- **CKY generation**

Since CWB (8V in CW mode) is 0V in any mode other than CW, Q64 is turned off, Q44 a/2 is turned on, and the base of Q50 is grounded. Q50 is turned on, and a high signal from the collector of Q49 passes through the collector of Q50, D61, R316, and pin 5 of the BK-IN module (X59-3870-00), and enters pin 2 of IC2 c/4 in the module.

The high output signal from Q50 enters pin 5 of the DLY module, and pin 12 of the IC1 one-shot multi-vibrator in the module goes high. The $\overline{Q}$ output from pin 9 of IC1 is low for 10 ms, then goes high. The $\overline{Q}$ output enters pin 1 of IC2 C/4 in the module via pin 4 of the DLY module and pin 4 of the BK-IN module. Pin 3 of IC2 C/4 goes low 10 ms after the standby switch is pressed. The signal is inverted by inverter IC2 d/4, and is output from pin 9 of the module as the CKY signal.

The CKY signal then passes through the integration circuit, which rectifies the waveform, is directed to the ALC line, matched with the negative signal of the ALC, and used as the FET gate bias of the transmit IF stage.

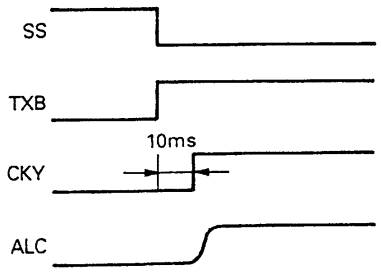


Fig. 13 TXB and CKY generation

- **Transmission → Reception**

When the standby switch is turned off, Q49 is turned off, and pin 10 of the BK-IN module goes low. Output from pin 4 of IC1 (b/6) is delayed 5ms after the standby switch is turned off because of the time constant circuit consisting of R1 and C1 between pin 2 of IC1 a/6 and pin 3 of b/6. Pin 2 of the TRX module goes low via pin D1 and D2 in the module. Therefore, TXB goes low 5 ms after the standby switch is turned off, and RXB goes high.

- **CKY down**

When the standby switch is turned off, the collector of Q50 goes low and pin 5 of the BK-IN module goes low. This causes the CKY line to go low at the same time. The CKY signal then passes through the integration circuit, which rectifies the waveform and reduces the ALC line voltage.

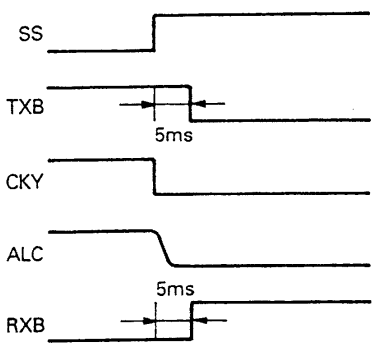


Fig. 14 TXB and CKY down

CIRCUIT DESCRIPTION

• **RBC generation**

When pin 2 of the BK-IN module goes low, pin 11 of IC1 e/6 and pin 13 of f/6 in the module go low. Because of the time constant circuit consisting of R5 and C3, the output from pin 10 of IC2 a/4 goes low 12.5ms after the standby switch is turned off, producing the RBC signal.

The RBC signal is applied to the base of the switching transistor that mutes the signal line of the IF unit. The signal is output to the signal line 12.5ms after the standby switch is turned off.

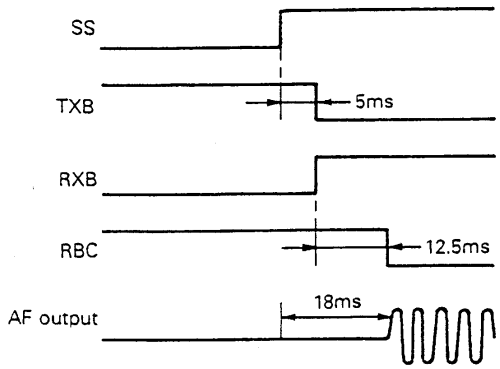


Fig. 15 RBC generation

• **PLL, DDS data and transmit/receive timing signal**

It takes 10ms from the time the standby switch is grounded until the CKY signal is generated. It takes 12.5ms from the time RXB rises until the RBC line goes low. The PLL and DDS data from the microprocessor are switched, and the diode switch and analog switch are switched during that time to assure stable transmission and reception.

2) Full break-in operation timing

• **TXB generation by closing the CW key**

When a key is inserted into the jack, the switch in the jack is closed, the junction of R262 and R261 goes low, and Q44 is turned off.

When the key is depressed, the base of Q34 is grounded through R264 and D51, Q34 is turned on, and a high signal from CWB enters pin 8 of IC1 through the collector of Q34, D54, and pin 2 of the BK-SW module. The FULL/SEMI switch is grounded during full break-in, the switch for pins 8 and 9 of IC1 is turned on, and a high signal is output from pin 9 and enters pin 10 via D1. Since the VOX switch is also turned on during full break-in, pin 5 of the BK-SW module connected to the VOX switch goes high. The switch for pins 10 and 11 of IC1 are turned on, and Q3 connected to pin 11 of IC1 is turned on. If the TXI signal is high, Q49 is turned on, as in manual standby, and a high signal enters pin 10 of the BK-SW module from the collector of Q49 and exits from pin 2. Pin 2 of the TRX module goes high, and the TXB signal is generated.

• **CKY generation**

When the key is depressed, the collector of Q34 goes high, and Q44 is turned on via D40. Both Q49 and Q50 are turned on, and a high signal enters pin 5 of the BK-IN module through D61 and R316. The CKY signal rises 10 ms after the key is depressed in the same manner as for CKY generation at manual standby.

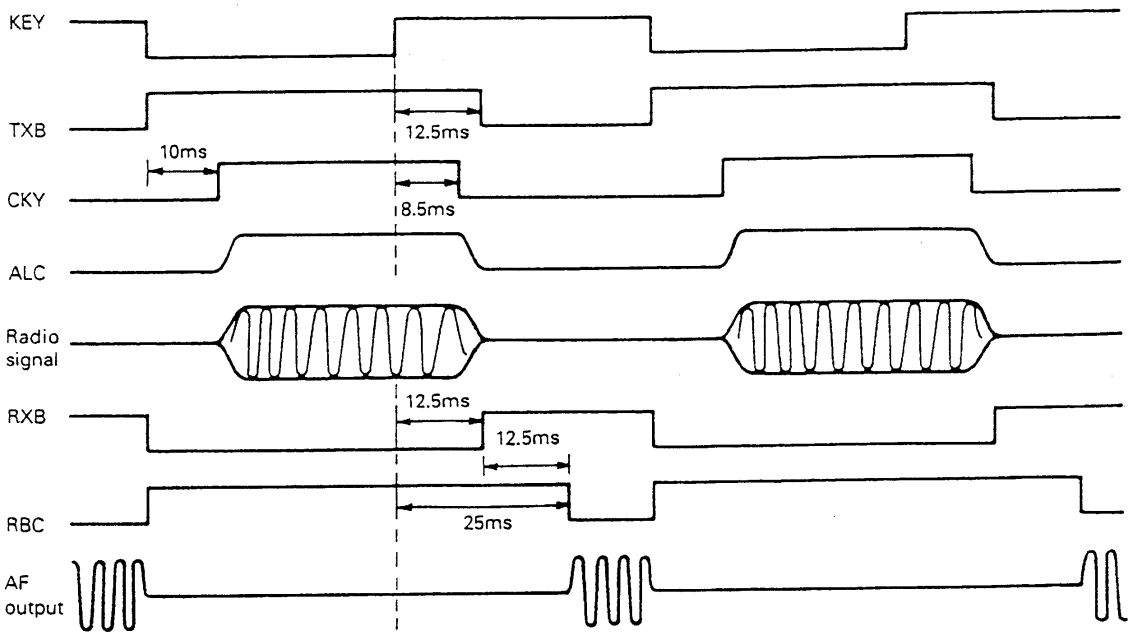


Fig. 16 Timing chart for full break-in

TS-850S

CIRCUIT DE

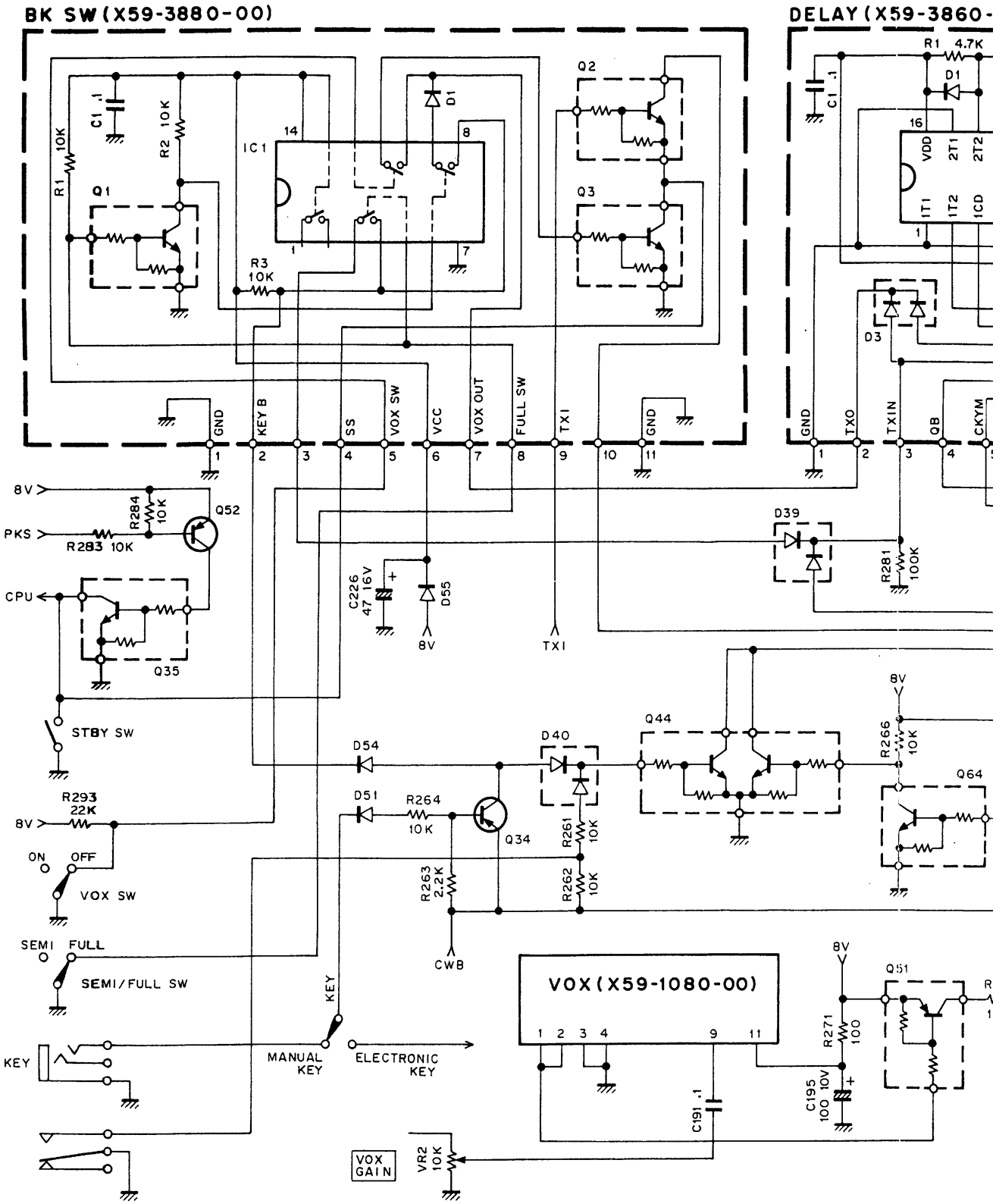
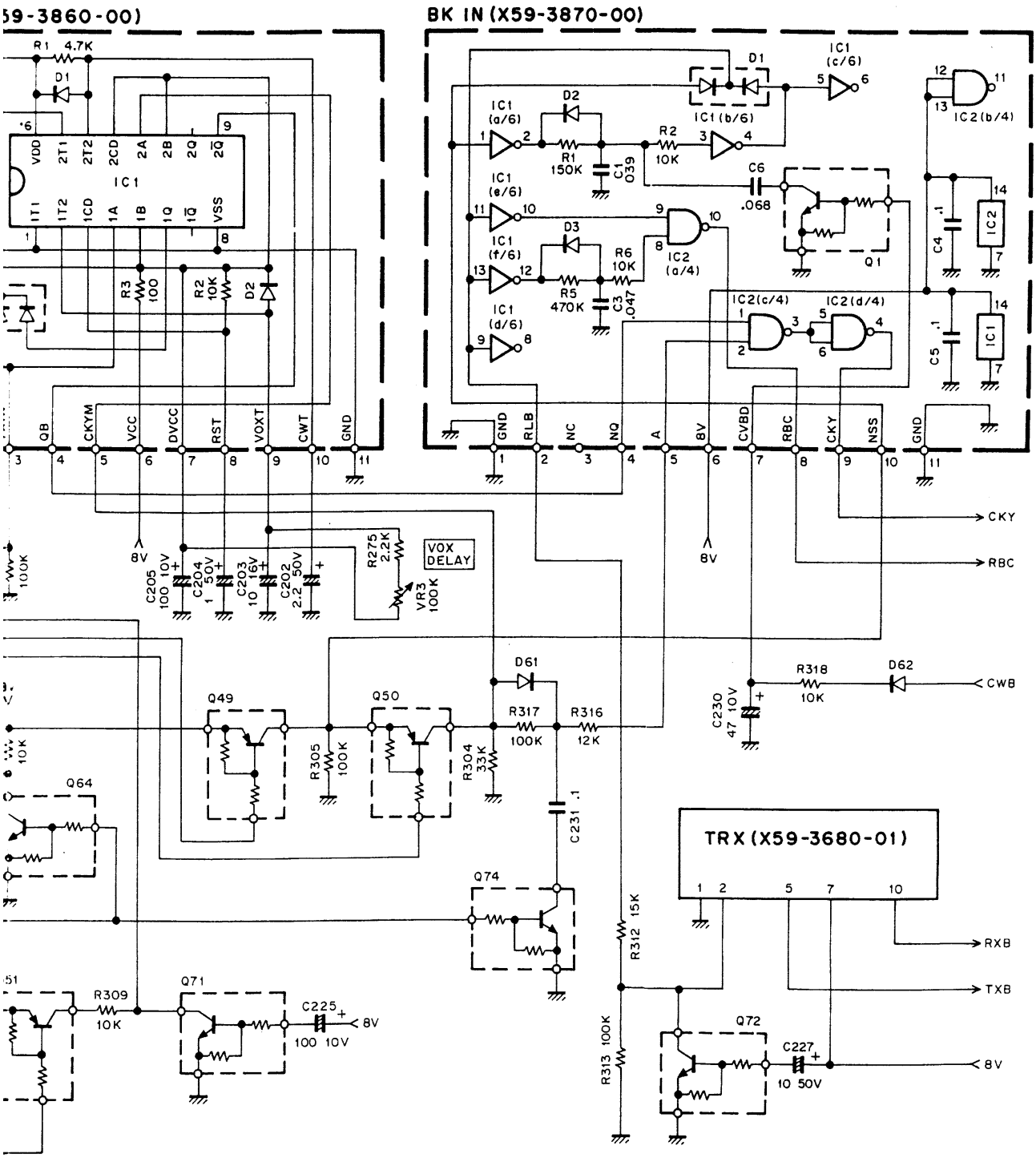


Fig. 17 Standb

0S TS-850S

UIT DESCRIPTION



17 Standby timer circuit

CIRCUIT DESCRIPTION

• **Key up**

When the key is up, pin 10 and pin 2 of the BK-IN module go low. TXB goes low, and RXB goes high. This differs from manual standby non-CW operation, since the signal passes from CWB in the CW mode through D62, R318, and pin 7 of the BK-IN module to turn on Q1. C6 is connected in parallel with C1, and the TXB delay time when the key is up is 12.5ms.

There is a switch circuit consisting of C230 and Q74 between D61 and R316 for the CKY output for Q50. In CW mode, Q74 is turned on, and C230 enters the output side of R317 to produce the necessary delay on key up. The time constant generated by the RC circuit is used to provide a correction of about 8.5ms when the key is up by raising the CKY waveform 10ms after the key is depressed to prevent deterioration of the waveform.

• **RXB and RBC generation**

TXB changes from high to low, and RXB goes high 12.5ms after the key is up.

RBC operates the receive signal line with a delay of 12.5ms in the same way as for manual standby.

3) Timing for semi break-in operation

• **TXB generation by key down**

When the key is down, Q34 is turned on, and a high signal enters pin 2 of the BK-SW module via D54 in a similar manner as previously described for full break-in.

When the SEMI/FULL switch is set to semi break-in, pin 8 of the BK-SW module goes high, pin 5 of IC1 in the module goes high, and the switch for pins 3 and 4 of IC1 is turned on.

A high signal from D54 is output from pin 3 of the module via pins 4 and 3 of IC1, and enters pin 3 of the DLY module. This high signal makes pin 4 of IC1 in the module, terminal A of the one-shot multi, high. A constant high signal is output from the Q output from pin 6. The pulse width of the one-shot multi-vibrator can be varied with the VOX delay VR, and the time is the same as the delay time for VOX operation. The Q output of IC1 passes through D3, is output from pin 2, and enters pin 7 of the BK-SW module.

When VOX is on, pins 10 and 11 of IC1 in the module are turned on, the base of Q3 goes high, and Q49 is turned on in the samemanners as previously described for full break-in to produce the basis for TXB. The CKY signal rises after a delay of 10ms in the same manner as for full break-in. The CKY signal rises after a delay of 8.5ms when the key is raised.

4) Standby from the data communication terminal

When the PKS terminal is grounded, Q52 and Q53 are turned on, and the SS line is grounded. Subsequent operations are the same as for manual standby in modes other than the CW mode.

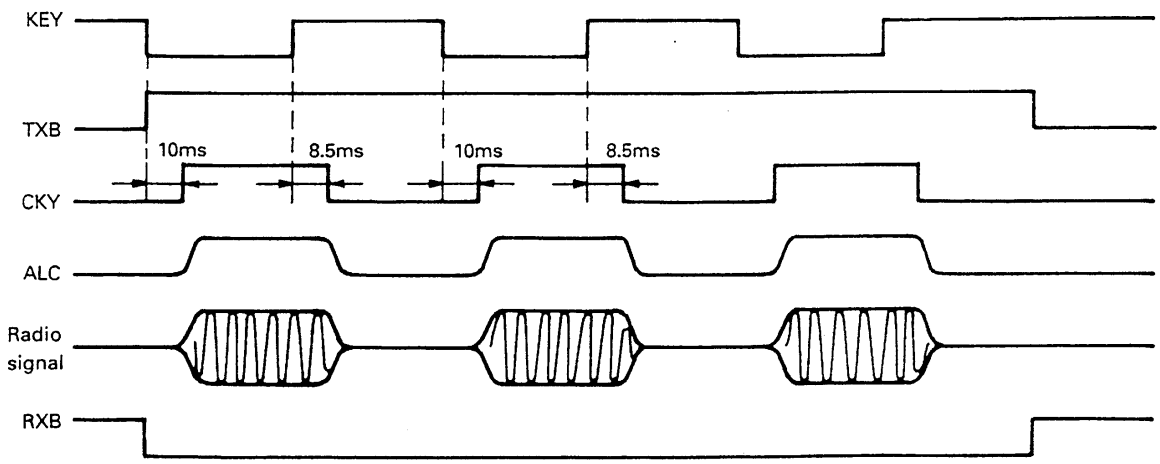


Fig. 18

CIRCUIT DESCRIPTION

Digital Control Unit

The TS-850 digital control circuit has a multiple chip configuration centered around IC6 (μPD78C10G), and consists of a 32K ROM (IC18, M27C256B), an 8K RAM (IC13, TC5564APL), and an I/O port (IC1, IC3, MB89363B; IC2, CXD1095Q). This circuit controls about 50 different inputs and about 90 different outputs.

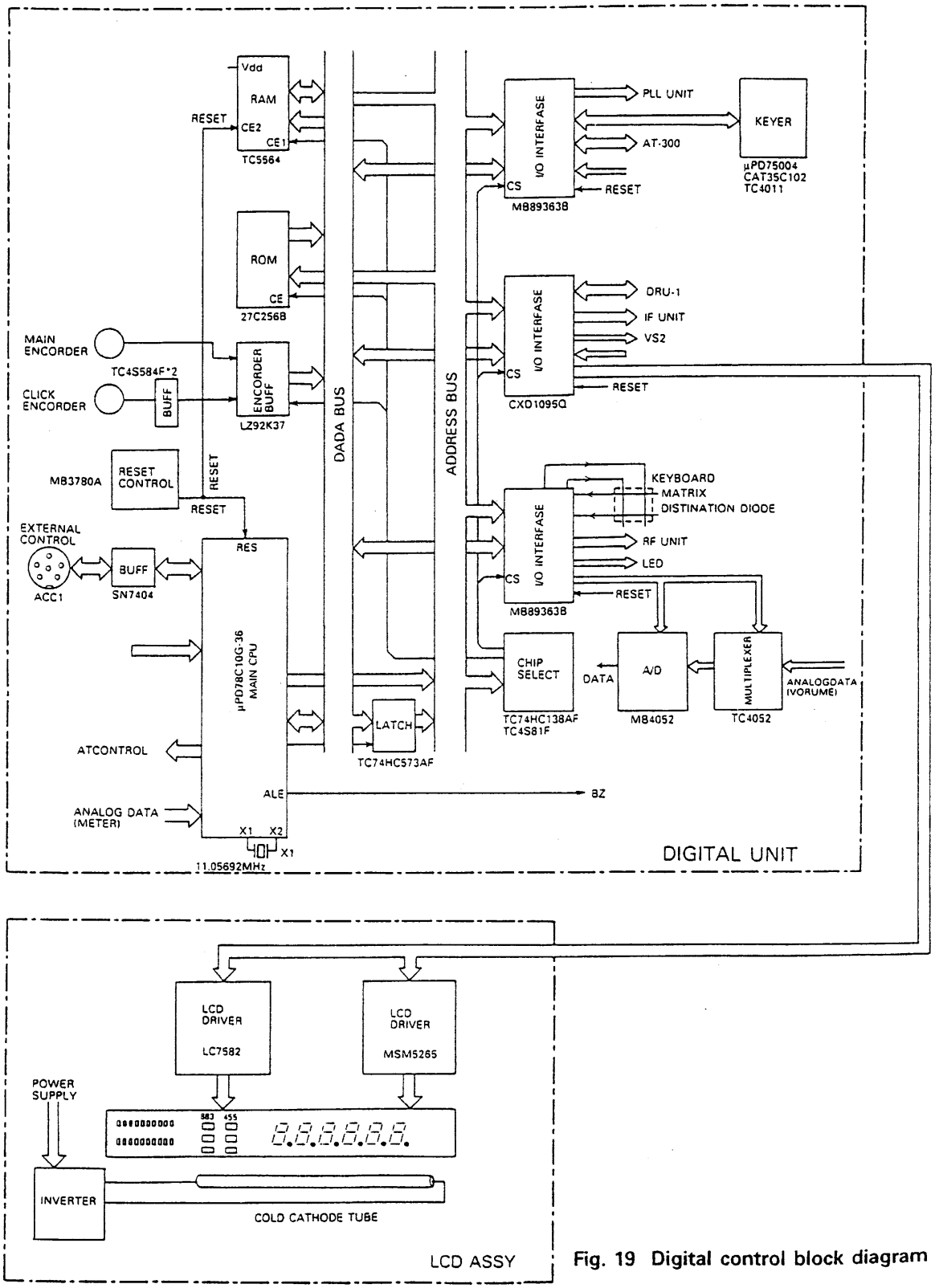


Fig. 19 Digital control block diagram

CIRCUIT DESCRIPTION

1) Encoder circuit

The main encoder is a magnetic rotary encoder, and the click encoder is a contact-type rotary encoder.

Encoder pulses are applied to the gate array (IC14, LZ92K37), and read via the CPU bus. The gate array is selected by the Y3 line. Encoder CK1, CK2, or CK3 is selected by A0. Encode data is output to D0 to D7 by making RD active when the chip select signal is active. IC15 and IC16 are used to rectify the waveform of the click encoder pulses.

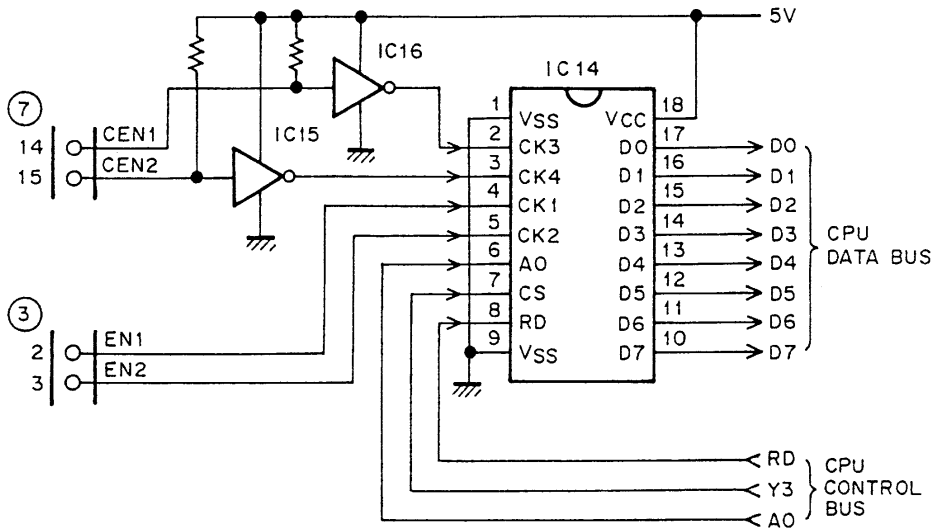


Fig. 20 Encoder circuit

2) System reset, RAM backup

The power supply voltage is detected by the power monitor IC (IC23, MB3780A). If the voltage is low, the IC outputs a RESET signal to the CPU and I/O port to stop operation and provide back up voltage to the RAM with an internal lithium battery.

When the power supply voltage returns to normal (including power on), the reset is released, the CPU and I/O port are initialized after the time constant set by C302, and operation resumes. The power to the RAM is supplied from the outlet.

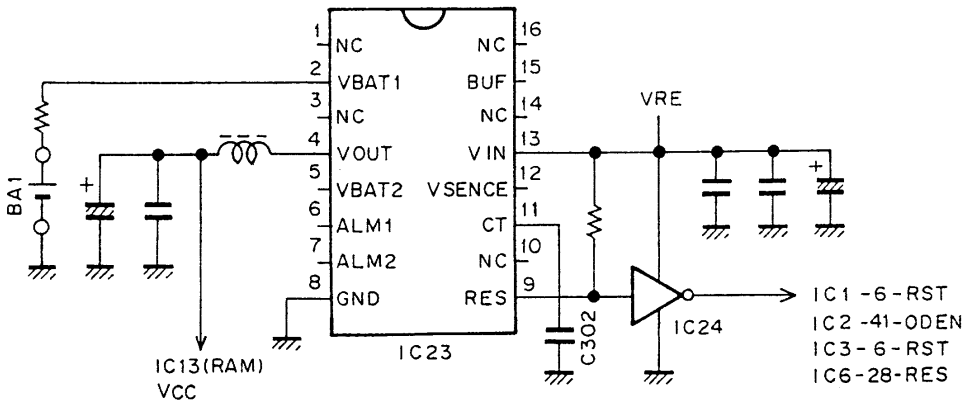


Fig. 21 System reset and RAM backup

CIRCUIT DESCRIPTION

3) Address control

Since PD0 to PD7 of the main CPU have multiplexed address and data signals, the address signal is separated from the data signal by latching the address signal using the ALE signal from IC10 (TC74HC573AF). PF0 to PF7 become the high-order byte of the address.

The address signal of A12 to A15 is used as a chip select signal for each IC by address decoder IC11 (TC74HC138AF).

Memory Map

0000	ROM	IC18 : M27C256B
8000	I/O	IC3 : MB89363B
A000	I/O	IC2 : CXD1095Q
B000	Encoder	IC14 : LZ92K37
C000	I/O	IC1 : MB89363B
E000	RAM	IC13 : TC5564APL
FFFF		

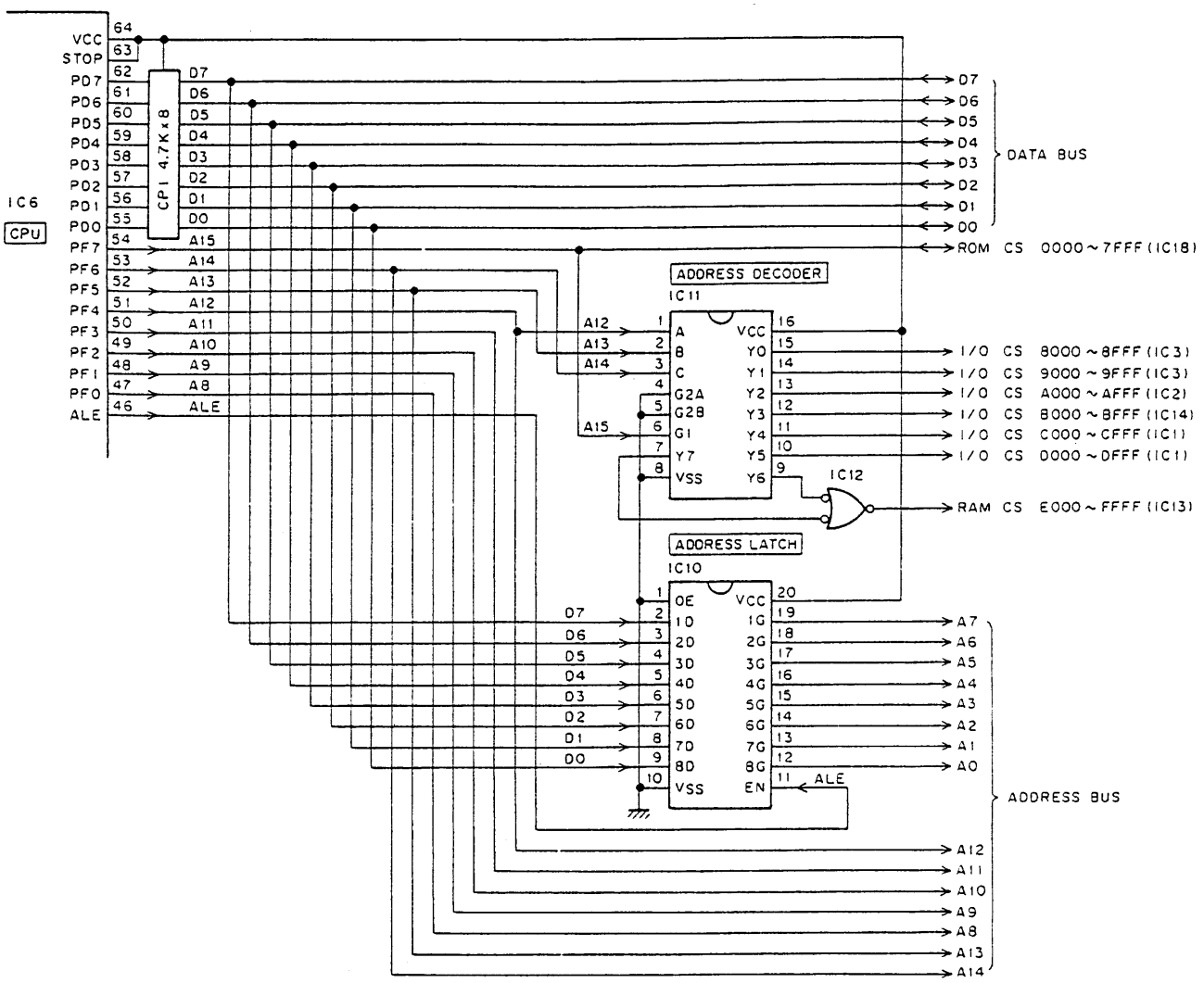


Fig. 22 Address control

CIRCUIT DESCRIPTION

4) Analog signal input

The main microprocessor incorporates an 8-channel analog-to-digital (A/D) converter, and in addition, has IC4 (MB4056) (A/D) and IC5 (analog switch) for entering 14-channel analog signals. Incoming analog signals are converted to digital values, which are used as digital signals.

IC6 : μPD78C10G (CPU)

Port	Signal	Description
AN0	ALM	ALC meter control voltage
AN1	SM	S-meter control voltage
AN2	CPM	Processor meter control voltage
AN3		Not used
AN4	VSRM	SWR meter control voltage
AN5		Not used
AN6	VSFM	RF meter control voltage
AN7		Not used

IC4 : MB4052 (A/D converter)

Port	Signal	Description
A0	CRU2	USB carrier point control voltage
	CRW2	Window alignment carrier control voltage
	CRL2	LSB carrier point control voltage
	POD2	AT variable capacitor 2 position control voltage
A1	LC2	Slope tune low-cut control voltage
	HC2	Slope tune high-cut control voltage
	RIT2	RIT/XIT control voltage
	POD1	AT variable capacitor 1 position control voltage
A2		Not used
A3	RMC2	Wired remote controller voltage

IC5 (TC4052) switches between the A0 and A1 signals.

5) Display

The TS-850 uses a transmission-type display with a negative LCD and a cold cathode tube. The LCD is lit by the LCD driver with a 50% duty cycle. The cold cathode tube is lit by the inverter, and the dimmer is operated by changing the duty cycle of the inverter. Data for the LCD driver is set by the clock (LCK), data (LDA), and enable (LEN1, LEN2) signals. The switching on and off of the LCD driver is controlled by BLK and INH.

6) PLL and DDS data

The TS-850 has 2 PLLs and 4 DDSs. The main microprocessor provides data to the PLL's and DDS's according to the displayed frequency. Ten PLL IC's provide unlock data signals. If one of the PLL's should unlock, the display indicates that the PLL is unlocked.

7) Key scan

The P1X port and P2X port of IC3 form a keyboard matrix. A key scan signal (a negative pulse) is output from the P2X port. One column corresponding to the P1X port is selected, and the state of that switch is read. When the switch at the intersection of the matrix is pressed, the P1X port bit goes low. Thus, which switch is pressed can be detected. The keys are software debounced.

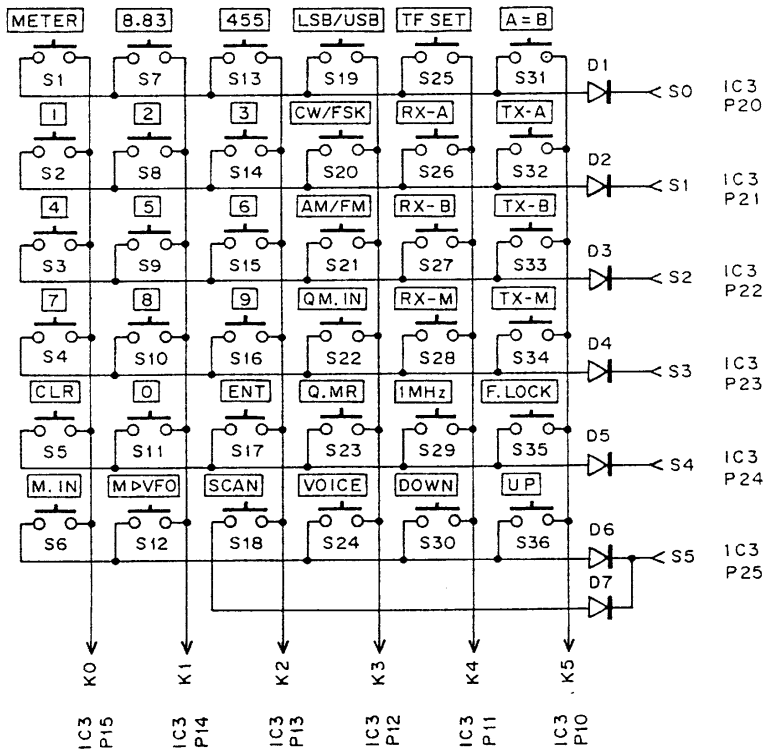


Fig. 23 Key-scan

CIRCUIT DESCRIPTION

8) AT control

The AT is controlled by the variable capacitor position data (POD1, POD2, analog data input), motor normal/reverse rotation control (PR11, PR12, PR21, PR22), motor speed control (SPED), motor control switching (APRE), progressive wave for SWR calculation, and reflected wave voltage (VSFM, VSRM analog data input).

SPED controls the switching on and off of the motor rotation during AT tune and presetting by PWM with the duty cycle related to the SWR value.

APRE changes the motor normal/reverse rotation control to analog control for AT tune, and to digital control for presetting.

PR performs the motor normal/reverse rotation control and stop control when the motor normal/reverse control is performed digitally.

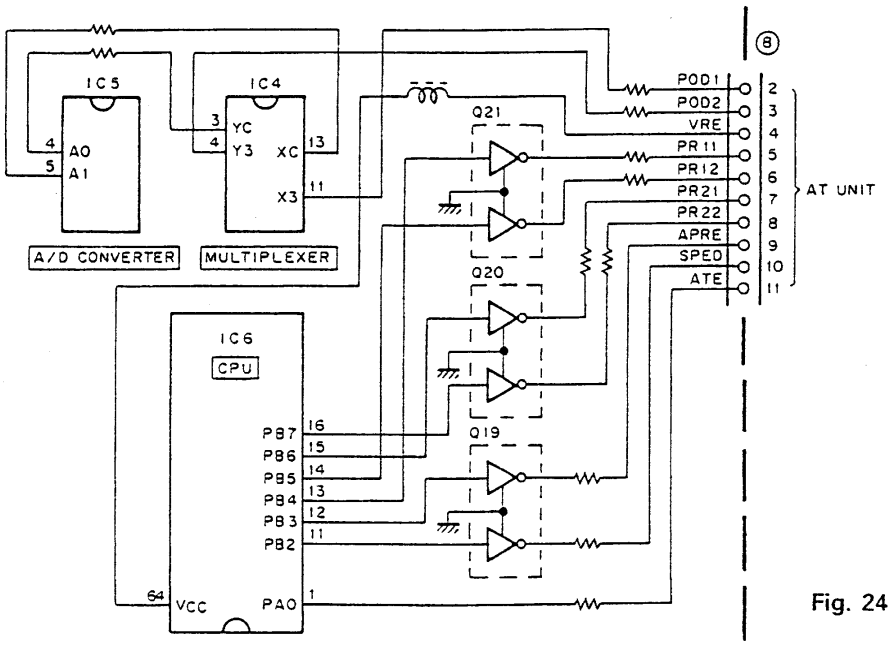


Fig. 24 AT control

9) IF filter switching

The IF filter switching signal from the digital unit is sent to the RF unit as 10-bit serial data. In the RF unit, serial-to-parallel converter IC8 (TC9174F) converts the serial data to parallel data to select the 8.83-MHz filter and the 455-kHz IF filter.

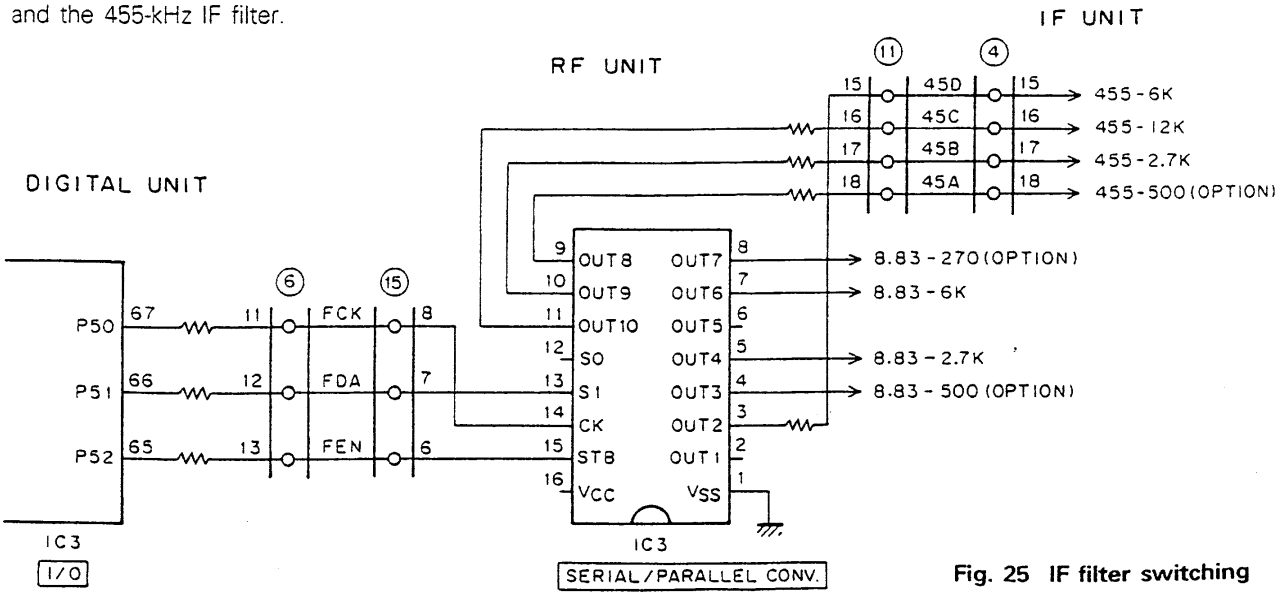


Fig. 25 IF filter switching

CIRCUIT DESCRIPTION

10) Receive band-pass filter selection

The RF BPF signal (RB0 to RB3) from the digital unit is buffered by Q5 and Q6 of the digital unit, then forwarded to the RF unit. The RF unit obtains the RF BPF data using BCD-to-decimal decoders.

11) Transmit low-pass filter, AT band data

Transmitter system band data (TB0 to TB3) from the digital unit is buffered by Q10 and Q11 of the digital unit, then forwarded to the filter unit. The filter unit obtains TX LPF data and AT band data using BCD-to-decimal decoders.

12) PLL VCO data

The PLL unit switches the VCOs according to the VCO band data (VB0 to VB3) from the digital unit.

13) Electronic keyer control

The electronic keyer microprocessor is controlled by transferring 8-bit commands serially. The commands include automatic electronic keyer correction, automatic correction reversal, bug key mode setting, manual weight setting, and recording/playback setting.

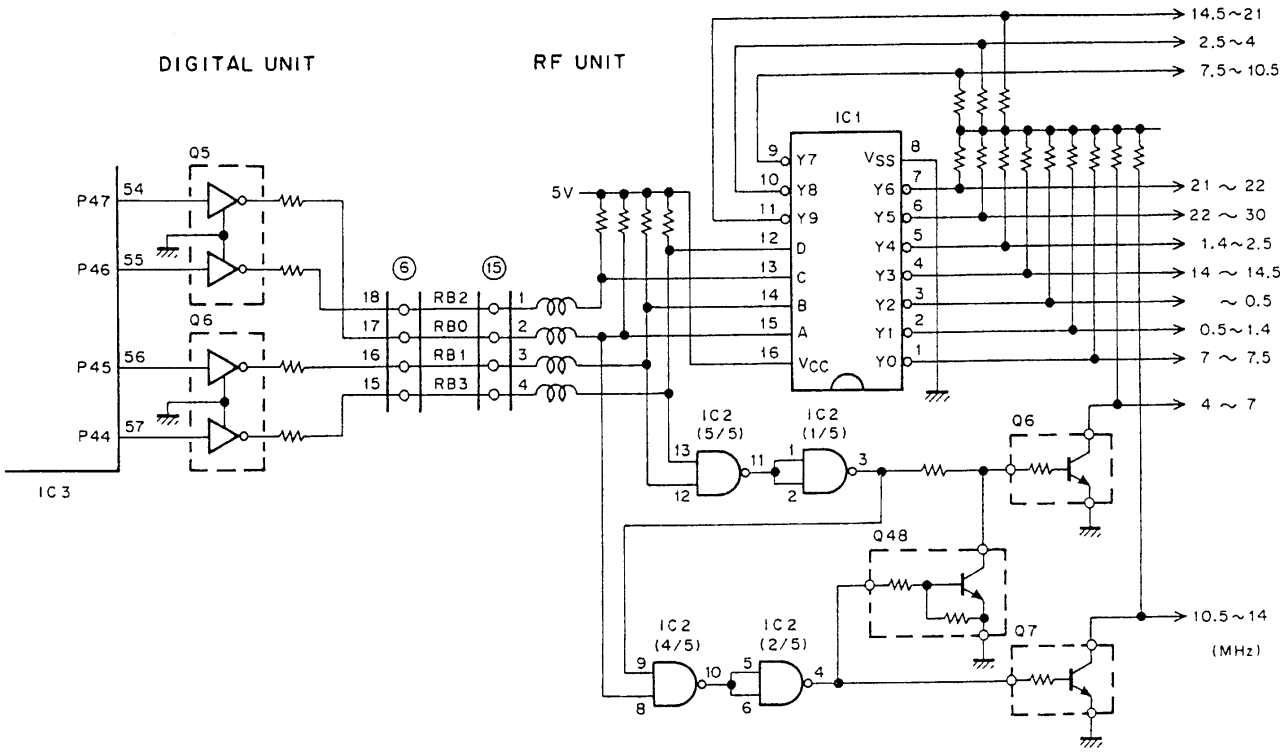


Fig. 26 Receiving BPF selection

14) Band data list

Frequency (MHz)	VB VCO-B				RB RX BPF				TB TX LPF			
	VB3	VB2	VB1	VB0	RB3	RB2	RB1	RB0	TB3	TB2	TB1	TB0
0.030000~ 0.499999	0	0	0	1	1	1	0	1	1	1	1	1
0.500000~ 0.999999	0	0	0	1	1	1	1	0	1	1	1	1
1.000000~ 1.499999	0	0	0	1	1	1	1	0	1	1	1	1
1.500000~ 1.620009 1.500000~ 1.705009 : K	0	0	0	1	1	1	1	0	1	1	1	1
1.620010~ 1.999999 1.705010~ 1.999999 : K	0	0	0	1	1	0	1	1	1	1	1	1
2.000000~ 2.499999	0	0	0	1	1	0	1	1	1	1	0	1
2.500000~ 2.999999	0	0	0	1	0	1	1	1	1	1	0	1
3.000000~ 3.499999	0	0	0	1	0	1	1	1	1	1	0	1
3.500000~ 3.999999	0	0	0	1	0	1	1	1	1	1	0	1

Note : VB, RB, and TB are logical values for the output pins of the I/O ports.

CIRCUIT DESCRIPTION

Frequency (MHz)	VB VCO-B				RB RX BPF				TB TX LPF			
	VB3	VB2	VB1	VB0	RB3	RB2	RB1	RB0	TB3	TB2	TB1	TB0
4.000000~ 4.499999	0	0	0	1	0	1	0	1	1	0	1	0
4.500000~ 4.999999	0	0	0	1	0	1	0	1	1	0	1	0
5.000000~ 5.499999	0	0	0	1	0	1	0	1	1	0	1	0
5.500000~ 5.999999	0	0	0	1	0	1	0	1	1	0	1	0
6.000000~ 6.499999	0	0	0	1	0	1	0	1	1	0	1	0
6.500000~ 6.999999	0	0	0	1	0	1	0	1	1	0	1	0
7.000000~ 7.499999	0	0	0	1	1	1	1	0	1	0	1	0
7.500000~ 7.999999	0	0	1	0	1	0	0	0	0	1	1	1
8.000000~ 8.499999	0	0	1	0	1	0	0	0	0	1	1	1
8.500000~ 8.999999	0	0	1	0	1	0	0	0	0	1	1	1
9.000000~ 9.499999	0	0	1	0	1	0	0	0	0	1	1	1
9.500000~ 9.999999	0	0	1	0	1	0	0	0	0	1	1	1
10.000000~10.499999	0	0	1	0	1	0	0	0	0	1	1	1
10.500000~10.999999	0	0	1	0	0	1	0	0	1	1	1	0
11.000000~11.499999	0	0	1	0	0	1	0	0	1	1	1	0
11.500000~11.999999	0	0	1	0	0	1	0	0	1	1	1	0
12.000000~12.499999	0	0	1	0	0	1	0	0	1	1	1	0
12.500000~12.999999	0	0	1	0	0	1	0	0	1	1	1	0
13.000000~13.499999	0	0	1	0	0	1	0	0	1	1	1	0
13.500000~13.999999	0	0	1	0	0	1	0	0	1	1	1	0
14.000000~14.499999	0	0	1	0	1	1	0	0	1	1	1	0
14.500000~14.999999	0	1	0	0	0	1	1	0	1	1	0	0
15.000000~15.499999	0	1	0	0	0	1	1	0	1	1	0	0
15.500000~15.999999	0	1	0	0	0	1	1	0	1	1	0	0
16.000000~16.499999	0	1	0	0	0	1	1	0	1	1	0	0
16.500000~16.999999	0	1	0	0	0	1	1	0	1	1	0	0
17.000000~17.499999	0	1	0	0	0	1	1	0	1	1	0	0
17.500000~17.999999	0	1	0	0	0	1	1	0	1	1	0	0
18.000000~18.499999	0	1	0	0	0	1	1	0	1	1	0	0
18.500000~18.999999	0	1	0	0	0	1	1	0	1	0	1	1
19.000000~19.499999	0	1	0	0	0	1	1	0	1	0	1	1
19.500000~19.999999	0	1	0	0	0	1	1	0	1	0	1	1
20.000000~20.499999	0	1	0	0	0	1	1	0	1	0	1	1
20.500000~20.999999	0	1	0	0	0	1	1	0	1	0	1	1
21.000000~21.499999	0	1	0	0	1	0	0	1	1	0	1	1
21.500000~21.999999	1	0	0	0	1	0	0	1	1	0	0	1
22.000000~22.499999	1	0	0	0	1	0	1	0	1	0	0	1
22.500000~22.999999	1	0	0	0	1	0	1	0	1	0	0	1
23.000000~23.499999	1	0	0	0	1	0	1	0	1	0	0	1
23.500000~23.999999	1	0	0	0	1	0	1	0	1	0	0	1
24.000000~24.499999	1	0	0	0	1	0	1	0	1	0	0	1
24.500000~24.999999	1	0	0	0	1	0	1	0	1	0	0	1
25.000000~25.499999	1	0	0	0	1	0	1	0	1	0	0	0
25.500000~25.999999	1	0	0	0	1	0	1	0	1	0	0	0
26.000000~26.499999	1	0	0	0	1	0	1	0	1	0	0	0
26.500000~26.999999	1	0	0	0	1	0	1	0	1	0	0	0
27.000000~27.499999	1	0	0	0	1	0	1	0	1	0	0	0
27.500000~27.999999	1	0	0	0	1	0	1	0	1	0	0	0
28.000000~28.499999	1	0	0	0	1	0	1	0	1	0	0	0
28.500000~28.999999	1	0	0	0	1	0	1	0	1	0	0	0
29.000000~29.499999	1	0	0	0	1	0	1	0	1	0	0	0
29.500000~30.000000	1	0	0	0	1	0	1	0	1	0	0	0

Note : VB, RB, and TB are logical values for the output pins of the I/O ports.

CIRCUIT DESCRIPTION

15) Function of IC pins

- **CPU : μPD78C10G (IC6)**

Port	Pin No.	Name	Function	I/O	Remarks
PA0	1	ATE	Internal AT connection determination	I	"L"= AT connection
PA1	2	ATA	AT AUTO/THRU switch	I	"L"= AUTO
PA2	3	XITS	XIT switch	I	"L" = Switch on
PA3	4	RITS	RIT switch	I	"L" = Switch on
PA4	5	EAT	Internal/external AT changeover switch	I	"L" = External, "H" = Internal
PA5	6	PDE	100W/10W filter determination	I	"L" = 100W, "H" = 10W
PA6	7	PT	Temperature protection input	I	"H" = Protection on
PA7	8	DATA IN	MB4052 serial data input	I	
PB0, PB1	9, 10		Nou used		
PB2	11	SPED	Internal AT motor speed control	O	"H" = Motor on
PB3	12	APRE	Motor control analog/digital switching	O	"L" = Digital, "H" = Analog
PB4	13	PR11	Motor 1 rotation direction control	O	
PB5	14	PR12	Motor 1 rotation direction control	O	
PB6	15	PR21	Motor 2 rotation direction control	O	
PB7	16	PR22	Motor 2 rotation direction control	O	
PC0	17	TXD	Personal computer interface transmit data	O	
PC1	18	RXD	Personal computer interface receive data	I	
PC2	19	CTS	Personal computer interface transmit enable data	I	
PC3	20	RTS	Personal computer interface receive enable data	O	
PC4, PC5	21, 22		Not used		
PC6	23	BEEP	Beep output	O	
PC7	24		Not used		
AN0	34	ALM	ALC meter voltage	I	A/D input
AN1	35	SM	Signal meter voltage	I	A/D input
AN2	36	CPM	Processor meter voltage	I	A/D input
AN3	37		Not used	I	A/D input
AN4	38	VSRM	Reflected wave voltage	I	A/D input
AN5	39		Not used	I	A/D input
AN6	40	VSFM	RF meter (forward wave) voltage	I	A/D input
AN7	41		Not used	I	A/D input
PD0~PD7	55~62	AD0~AD7	CPU address/data multiplexed bus	I/O	
PF0~PF7	47~54	A8~A15	CPU high-order address bus	O	
RD	44	RD	Read signal	O	"L" = Acknowledge
WR	45	WR	Write signal	O	"L"= Acknowledge
ALE	46	ALE	Address/data separation signal	O	
NMI	25	NMI	Normal couple interrupt	I	Always "H"
INT1	26	INT1	External interrupt	I	Always "L"
M1, M0	27, 29	M1, M0	External memory mode	I	Always "H"
AVcc	43	AVcc	Power supply for A/D converter	I	
AVref	42	AVref	Reference power supply for A/D converter	I	
AVss	33	AVss	Ground for A/D converter		
X1, X2	30, 31	X1, X2	CPU clock crystal pin	I	
RES	28	RES	CPU reset pin	I	"L" = Reset
STOP	63	STOP	CPU stop pin	I	Always "H"

- **Extended I/O : MB89363B (IC1)**

Port	Pin No.	Name	Function	I/O	Remarks
P00	28	CWCK	Electronic keyer microprocessor data clock	O	
P01	27	CWDA	Electronic keyer microprocessor data	O	
P02, P03	26, 25		Not used		
P04, P05	23, 22		Not used		

CIRCUIT DESCRIPTION

Port	Pin No.	Name	Function	I/O	Remarks
P06	21	TS	External AT control	O	
P07	20	TT	External AT control	O	
P10~P12	44~46	DPS3~DPS1	Optional filter installation switch	I	"L" = Installed
P13	47	SBSY	VS-2 busy	I	"H" = Busy
P14	48	UNL	PLL unlock signal	I	"L" = Unlocked
P15	49	VCK	DRU-2 installation signal	I	"H" = Installed
P16	50	PRS	Processor switch	I	"H" = Switch on
P17	51	ATS	AT start switch	I	"L" = Switch on
P20	38	MEA	Electronic keyer recording/playback busy	I	"H" = Busy
P21	39		Not used		
P22	40	BSY	Electronic keyer data transfer busy	I	"H" = Busy
P23	43	DPS4	Optional filter installation switch	I	"L" = Installed
P24	37	KEY	Electronic keyer keying input	I	"L" = Key on
P25	36	DBC	External DSP power on signal	I	"L" = Power on
P26	35	TS	External AT control	I	
P27	34	TT	External AT control	I	
P30~P33	77~80		Not used		
P34	1	RDC	Receive DSP switching	O	"L" = Analog, "H" = DSP
P35	2	TDC	Transmit DSP switching	O	"L" = Analog, "H" = DSP
P36, P37	3, 4		Not used		
P40	61	CASL	DDS register selection	O	"L" = Receive, "H" = Transmit
P41	60	ABSL	DDS register selection	O	"L" = Receive, "H" = Transmit
P42	59	TOC	Repeater tone control	O	"L" = Tone on
P43~P46	58~55	VB0~VB3	VCO band data	O	
P47	54	TU8C	TU-8 control	O	
P50	67	PCK	PLL, DDS control data clock	O	
P51	66	PDA	PLL, DDS control data	O	
P52	65	DLE4	DDS control data enable	O	
P53	62	DLE3	DDS control data enable	O	
P54	68	DLE2	DDS control data enable	O	
P55	69	DLE1	DDS control data enable	O	
P56, P57	70, 71	PLE2, PLE1	PLL control data enable	O	
DB0~DB7	12~19	DB0~DB7	Data bus	I/O	
RD	76	RD	Read signal	I	"L" = Acknowledge
WR	5	WR	Write signal	I	"L" = Acknowledge
RES	6	RES	Reset signal	I	"L" = Reset
A0, A1	31, 32	A0, A1	Port select signal	I	
CS0	29	CS0	Chip select signal	I	"L" = P0X to P2X selected
CS1	75	CS1	Chip select signal	I	"L" = P3X to P5X selected

- Extended I/O : CXD1095Q (IC2)

Port	Pin No.	Name	Function	I/O	Remarks
PA0	54	VOA	DRU-2 control audio input/output switching	O	
PA1	55	VOB	DRU-2 control audio input/output switching	O	
PA2	56	RD	DRU-2 control command read	O	
PA3	59	WR	DRU-2 control command write	O	
PA4	60		Not used		
PA5	61	STR	VS-2 synthesis control	O	"H" = Audio synthesis
PA6	62	SCK	VS-2 control data clock	O	
PA7	63	SD	VS-2 control data	O	
PB0	64	EKS	Electronic keyer changeover switch	I	"L" = Electronic keyer on
PB1	3	MUP	Microphone up switch	I	"L" = Switch on
PB2	4	MDN	Microphone down switch	I	"L" = Switch on

CIRCUIT DESCRIPTION

Port	Pin No.	Name	Function	I/O	Remarks
PB3	5	SS	Transmit/receive control signal	I	"L" = Transmission
PB4	6	VOX	VOX switch	I	"H" = Switch on
PB5	7	FULL	FULL/SEMI switch	I	"L" = FULL, "H" = SEMI
PB6	8	AIPS	AIP switch	I	"L" = Switch on
PB7	9	TXB	Transmit B signal	I	
PC0	11	CWC	CW mode	O	"H" = Mode selected
PC1	12	TXI	Transmission inhibit signal	O	"H" = Transmission inhibit
PC2	13	RSS	Transmission request signal	O	"H" = Transmission request
PC3	14	AMC	AM mode	O	"H" = Mode selected
PC4	15	RYC	FSK mode	O	"H" = Mode selected
PC5	16	FMC	FM mode	O	"H" = Mode selected
PC6	17	SSBC	SSB mode	O	"H" = Mode selected
PC7	18	ABK	AF blanking	O	"H" = Blanking
PD0	20	LCK	LCD control data clock	O	
PD1	21	LDA	LCD control data	O	
PD2	22	INH	LCD all-off	O	
PD3	23	BLK	LCD all-off	O	
PD4	24	LEN2	LCD control data enable	O	
PD5	27	LEN1	LCD control data enable	O	
PD6, PD7	28, 29		Not used		
PE0, PE1	49, 50	D1, D2	DRU-2 control data	I/O	
PE2, PE3	52, 53	D4, D8	DRU-2 control data	I/O	
D0~D7	30~32, 35~39	D0~D7	Data bus	I	
RD	44	RD	Read signal	I	"L" = Acknowledge
WR	43	WR	Write signal	I	"L" = Acknowledge
A0~A2	46~48	A0~A2	Port select signal	I	
CS	45	CS	Chip select signal	I	
ODEN	41	ODEN	Output disable	I	When reset, all ports become input ports

- **Extended I/O : MB89363B (IC3)**

Port	Pin No.	Name	Function	I/O	Remarks
P00	28	AIL	AIP LED control	O	
P01	27	MHL	1MHz LED control	O	
P02	26	RXAL	Function LED control	O	
P03	25	RXBL	Function LED control	O	
P04	23	RXML	Function LED control	O	
P05	22	TXAL	Function LED control	O	
P06	21	TXBL	Function LED control	O	
P07	20	TXML	Function LED control	O	
P10~P15	44~49	K5~K0	Key matrix input	I	
P16, P17	50, 51		Not used		
P20~P22	38~40	S0~S2	Key matrix output	O	
P23	43	S3	Key matrix output	O	
P24~P26	37~35	S4~S6	Key matrix output	O	
P27	34	ATL	AT LED control	O	
P30, P31	77, 78	C1, C0	MB4052 channel selection	O	
P32	79	CS	MB4052 chip selection	O	
P33	80	CLK	MB4052 control clock	O	
P34	1	SELA	TC4052 channel selection	O	
P35	2	SELB	TC4052 channel selection	O	
P36, P37	3, 4		Not used		
P40~P43	61~58	TB0~TB3	TX LPF band data	O	

CIRCUIT DESCRIPTION

Port	Pin No.	Name	Function	I/O	Remarks
P44,P45	57,56	RB3,RB1	RX BPF band data	O	
P46,P47	55,54	RB2,RB0	RX BPF band data	O	
P50	67	FCK	Filter selection data clock	O	
P51	66	FDA	Filter selection data	O	
P52	65	FEN	Filter selection data enable	O	
P53	62	RBK	RF blanking	O	"H" = Blanking
P54	68	ATPD	AT power down	O	"H" = Power down
P55	69	TPD	TUNE power down	O	"H" = Power down
P56	70	BPD	BAND power down	O	"H" = Power down
P57	71	AIP	AIP control	O	"L" = AIP on
DB0~DB7	12~19	DB0~DB7	Data bus	I/O	
RD	76	RD	Read signal	I	"L" = Acknowledge
WR	5	WR	Write signal	I	"L" = Acknowledge
RES	6	RES	Reset signal	I	"L" = Reset
A0,A1	31,32	A0,A1	Port select signal		
CS0	29	CS0	Chip select signal	I	"L" = P0X to P2X selected
CS1	75	CS1	Chip select signal	I	"L" = P3X to P5X selected

- **Electronic keyer : μPD75P008GB (IC21)**

Port	Pin No.	Name	Function	I/O	Remarks
P00	32	DOT	Dot input	I	
P01	31	SCK	Electronic keyer control data clock	I	
P02	30	DLY	Delay change	I	
P03	29	SI	Electronic keyer control data	I	
P10	37	SP	Serial/parallel input change	I	"L" = Serial
P11	36	DSH	Dash input	I	
P12	35	SPD	Speed clock input	I	
P13	33	EKS	Electronic keyer changeover switch	I	"L" = Electronic keyer on
P20	43	KEY	Keyer output	O	"H" = Keyer on
P21	42	RWL	Write LED control	O	
P22	41	MEA	Electronic keyer recording/playback busy	O	"H" = Busy
P23	40	BSY	Electronic keyer data transfer busy	O	"H" = Busy
P30	26	MDI	EEPROM data input	I	
P31	25	MDO	EEPROM data output	O	
P32	24	MSK	EEPROM data clock	O	
P33	23	MCS	EEPROM chip select	O	
P40~P43	16~13	WL0~WL3	Weight LED control	O	
P50~P53	11~8	B0~B3	Parallel data input (Manual wait)	I	Not used during serial control
P60,P61	7,6	CH0,CH1	Parallel data input (Channel selection)	I	Not used during serial control
P62	5	STA	Parallel data input (Recording/playback start)	I	Not used during serial control
P63	4	RWS	Parallel data input (Command write)	I	Not used during serial control
P70	3	FUL	Parallel data input (Full break-in correction)	I	Not used during serial control
P71	2	BKY	Parallel data input (Bug key mode)	I	Not used during serial control
P72	1	REV	Parallel data input (Wait correction reversal)	I	Not used during serial control
P73	44	AUTO	Parallel data input (Auto wait)	I	Not used during serial control
P80	28	M4K	EEPROM size select input	I	
P81	27	ACT	Weight LED active	I	
XT1, XT2	18, 19	XT1, XT2	Sub-clock input	I	
RES	20	RES	Reset input	I	
X1, X2	21, 22	X1, X2	Clock input	I	

CIRCUIT DESCRIPTION

Setting the Extended Functions

1) Setting for full-Morse function

Every time you turn the POWER ON while pressing the VOICE key, the full-Morse function is turned ON/OFF alternatively.

- **Morse for each key**

AIP key	AON - AOF
8.83 key	TH8 - AM8 - SW8 - SN8 - CW8 (It does not function at repeat.)
455 key	TH4 - AM4 - SB4 - CW4 - CN4 (It does not function at repeat.) At FM, FW - FN (It does not function at repeat.)
REC1,2,3 key	R1BT, R2BT, R3BT
FINE key	FNON - FNOF
TUNE key	TNON - TNOF
CLR key	CL
ENT key	ETON - ETOF
1~9,0 key	1~9, 0
M.IN key	MSCR - MIN
MÆVFO key	MV
SCAN key	SCST - SCON
QUICK M.IN key	QMIN
QUICK MR key	QMRON - QMROF
A=B key	AEB
A,B,M.CH key	RXA, RXB, RXM, TXM, TXB, TXM
1MHz key	1MON - 1MOF
F.LOCK key	FLON - FLOF
DOWN key	DN (It does not function at repeat.)
UP key	UP (It does not function at repeat.)
RIT key	RTON - RTOF
XIT key	XTON - XTOF
AT TUNE key	ATST - ATED
PITCH key	PTON - PTOF
REV key	At CW, CWN - CER At FSK, FSKN - FSKR

2) Setting for adjustment mode

Turning on while pressing F.LOCK key enters the menu mode under the adjustment mode.

Pressing the CLR key in the adjustment mode terminates the menu mode under the adjustment mode.

No other operation than pressing the CLR key or turning on again brings termination.

- **Menu for adjustment mode**

Menu No.	Menu items	Status (Display)
00	CAR correction FSK pseudo SSB Possible FILTER exchange at transmission	
01	CAR-W correction Possible FILTER exchange at transmission	
02	0 adjustment for RIT/XIT volume	-1.28-1.27
03	WIDE adjustment for SLOPE TUNE HIGH CUT volume	-128-127
04	WIDE adjustment for SLOPE TUNE LOW CUT volume	-128-127
05	Forced ON/OFF for receiving DSP carrier	ON/OFF
06	Forced ON/OFF for transmitting DSP carrier	ON/OFF
	Full-ON of LCD	
	Full-OFF of LCD	
	LCD test 1	
	LCD test 2	
	LCD test 3	
	LCD test 4	

3) Setting the extended functions

Turning on while pressing the SCAN key + TX-M.CH key enter the menu mode for extended functions.

Pressing the CLR key in the menu mode of the extended functions terminates the menu mode of the extended functions.

No other operation than pressing the CLR key or turning on again brings termination.

The menu items of the extended functions are shown in the table.

- **Menu for extensive functions**

Menu No.	Menu items	Status (Display)	Initial status
00	Indicates checksum of ROM	Indicates checksum of ROM in the range of 0000-FFFF.	
01	Turns ON/OFF FILTER exchange at transmission	ON/OFF	OFF
02	Forced ON/OFF AT power down	ON/OFF	OFF
03	AT non-stop mode ON/OFF	ON/OFF	OFF
04	MODE, FILTER of band memory ON/OFF	ON/OFF	ON
05	Power ON; ON/OFF for HELLO Morse	ON/OFF	OFF
06	Turns ON/OFF LCD full-ON mode at power ON	ON/OFF	OFF
07	Turns ON/OFF DDS subtone	ON/OFF	ON
08		ON/OFF	OFF

Treat Construction

Model name	Treat	Mark	AT function	Model name	Treat	Mark	AT function
TS-850S	North America	K	○	TS-850S	Belgium	E3	○
		K2	-			E4	-
TS-850S	Australia	X	○	TS-850S	Other Areas	M	○
		X2	-			M2	-
TS-850S	Canada	P	○			M3	○ *
		P2	-			M4	- *
TS-850S	Europe	E	○				
		E2	-				

* : General coverage