



AKAI

DVD HOME THEATER SYSTEM

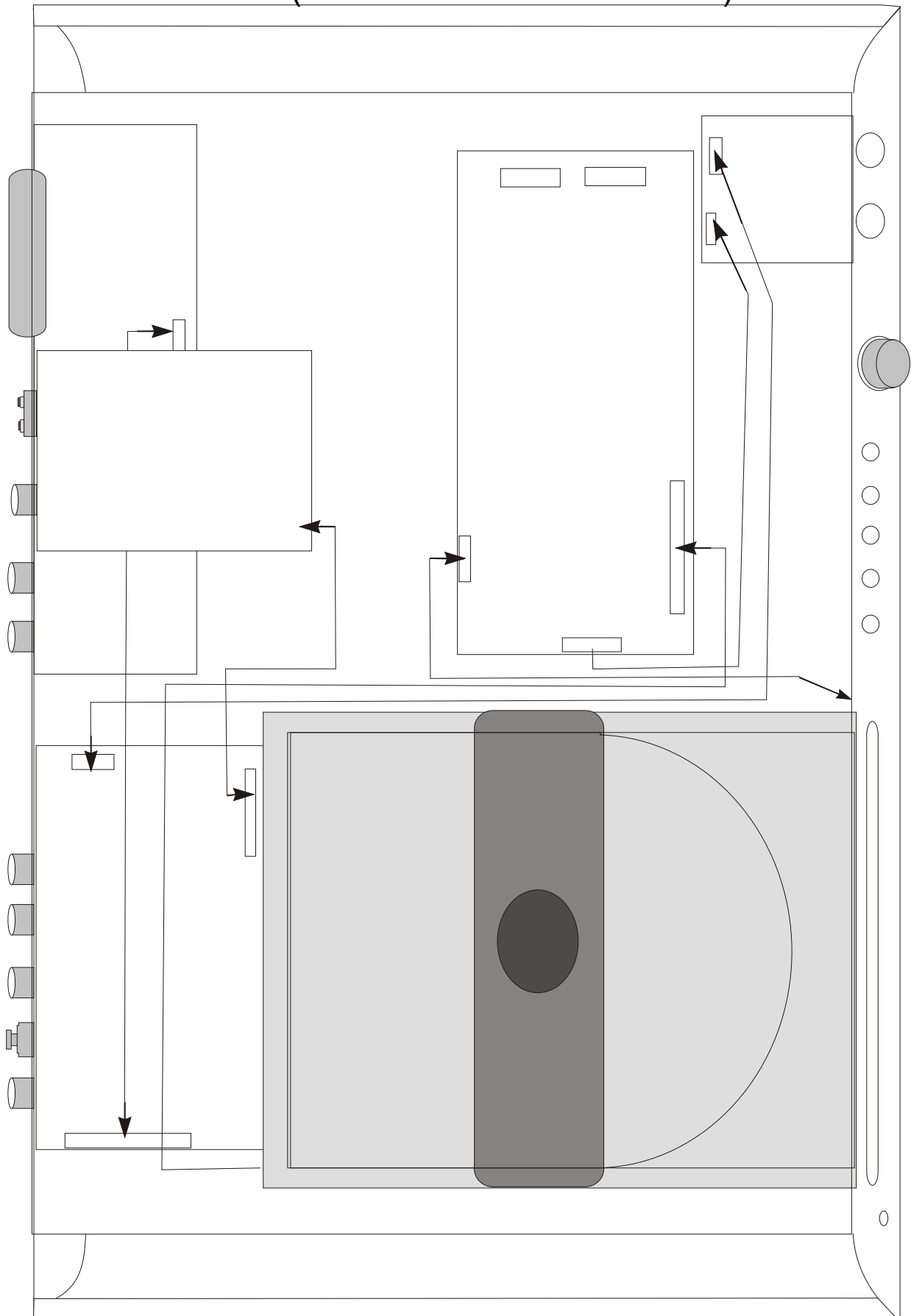
Model:
DV-R4025VSS

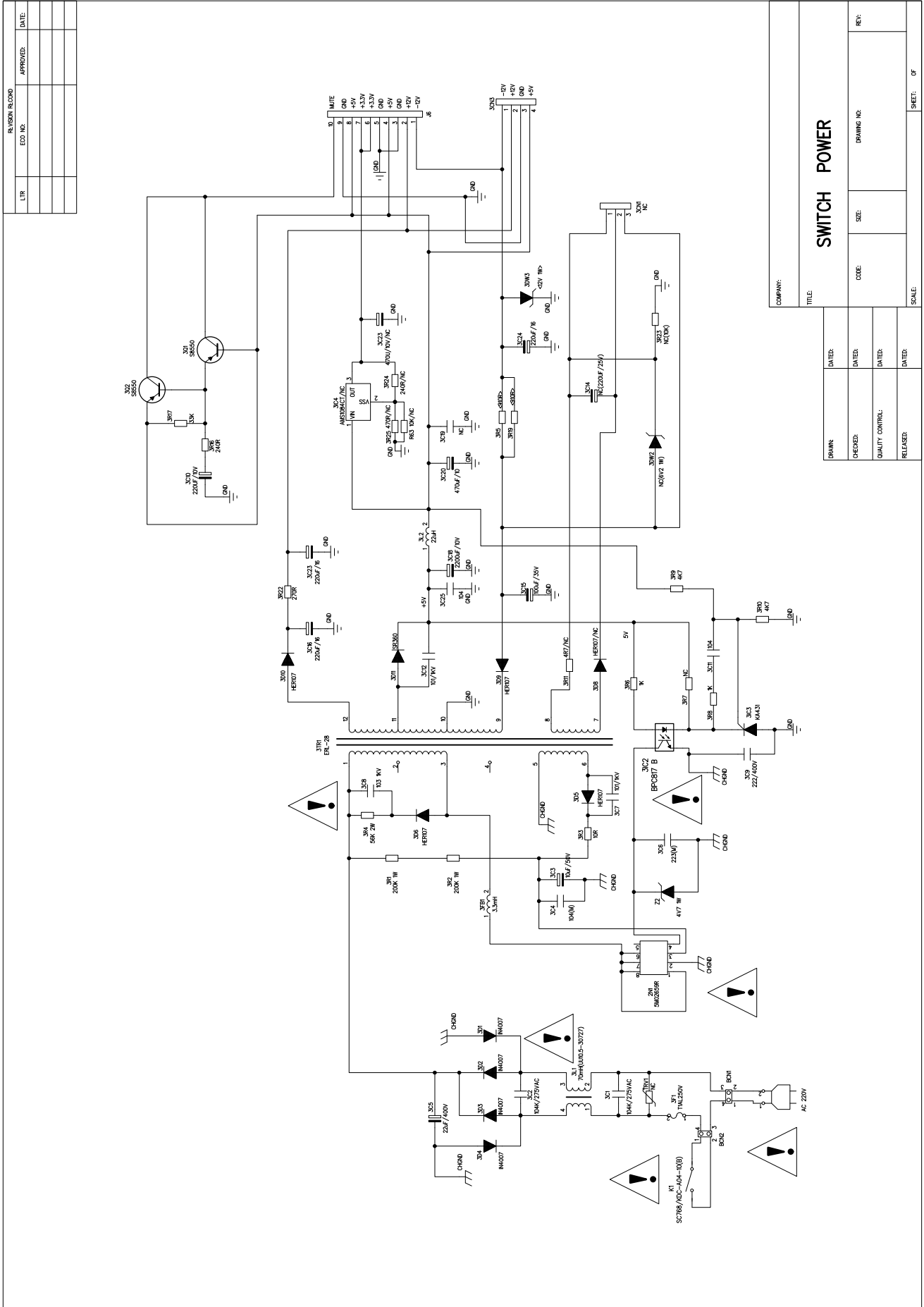
SERVICE MANUAL

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2. BLOCK DIAGRAM(CABLE CONNECTIONS)



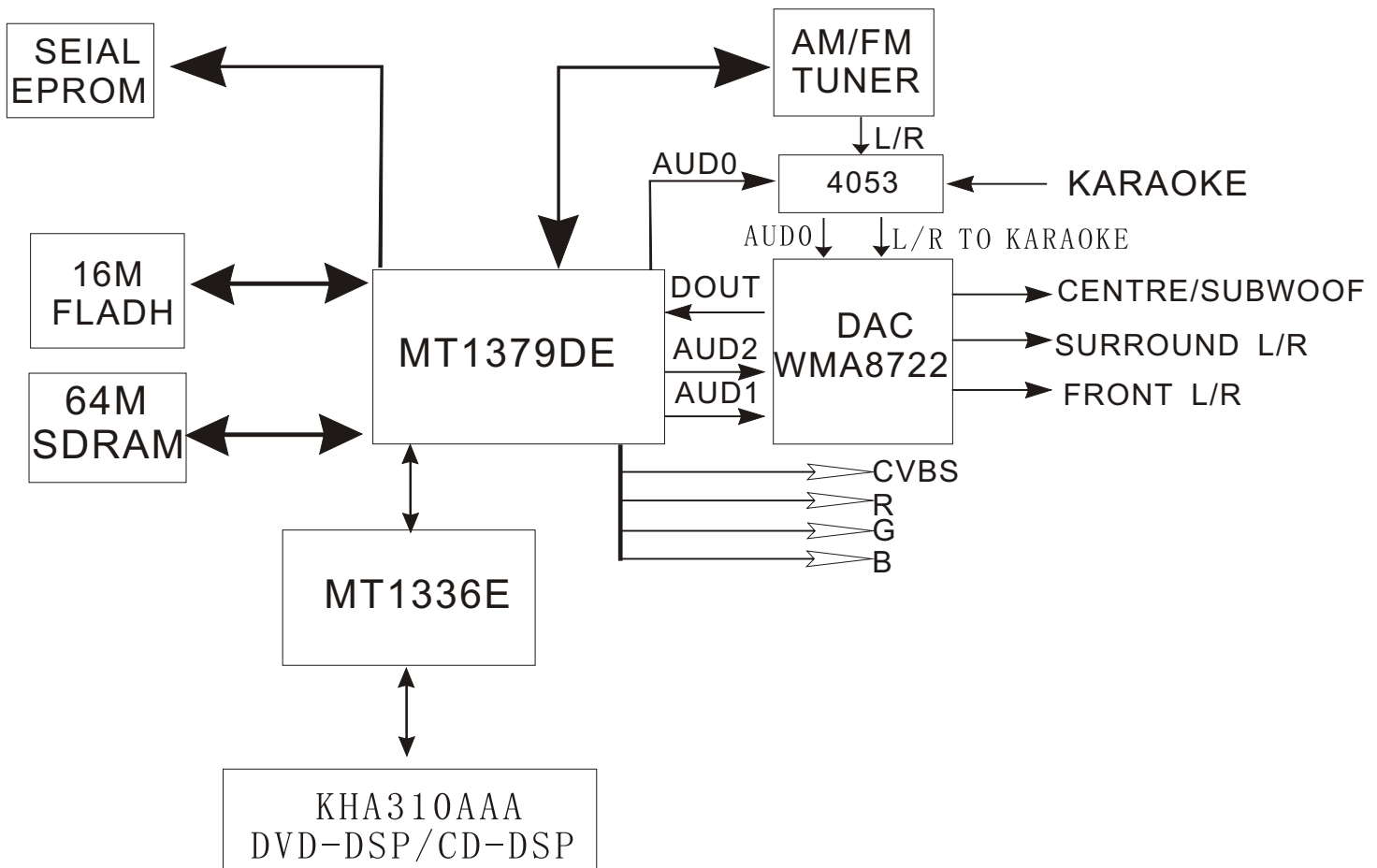


LT#	REVISION RECORD	APPROVED:	DATE:
	ECO NO.		

COMPANY:			
TITLE: SWITCH POWER			
DRAWN:	DATED:	CODE:	SIZE:
CHECKED:	DATED:	QUALITY CONTROL:	RELEASED:
DATED:	DATED:	DATED:	DATED:
DRAWING NO.:	SCALE:	SHEET:	OF

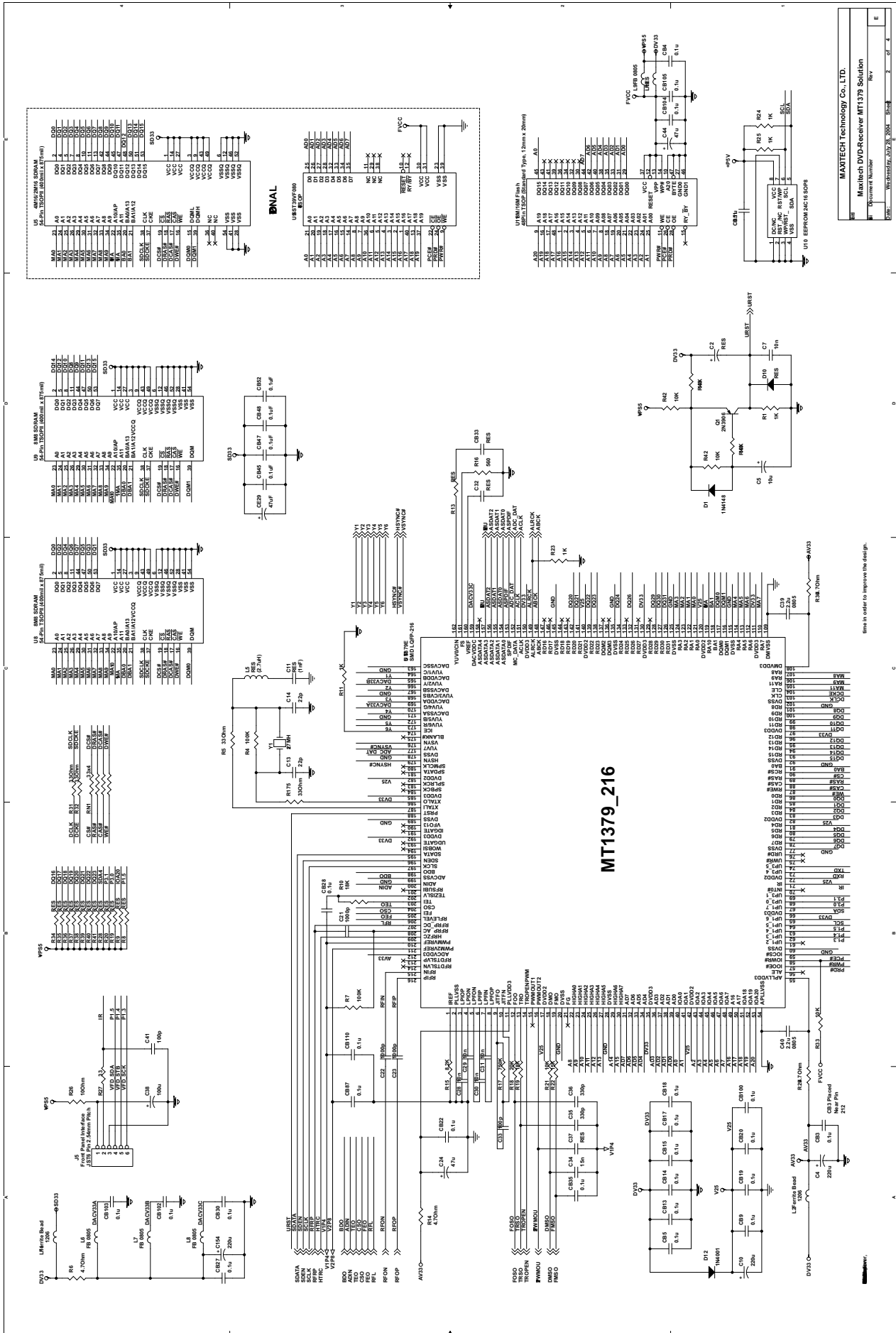
4. FUNCTIONAL DESCRIPTIONS

4.1 DVD MPEG board



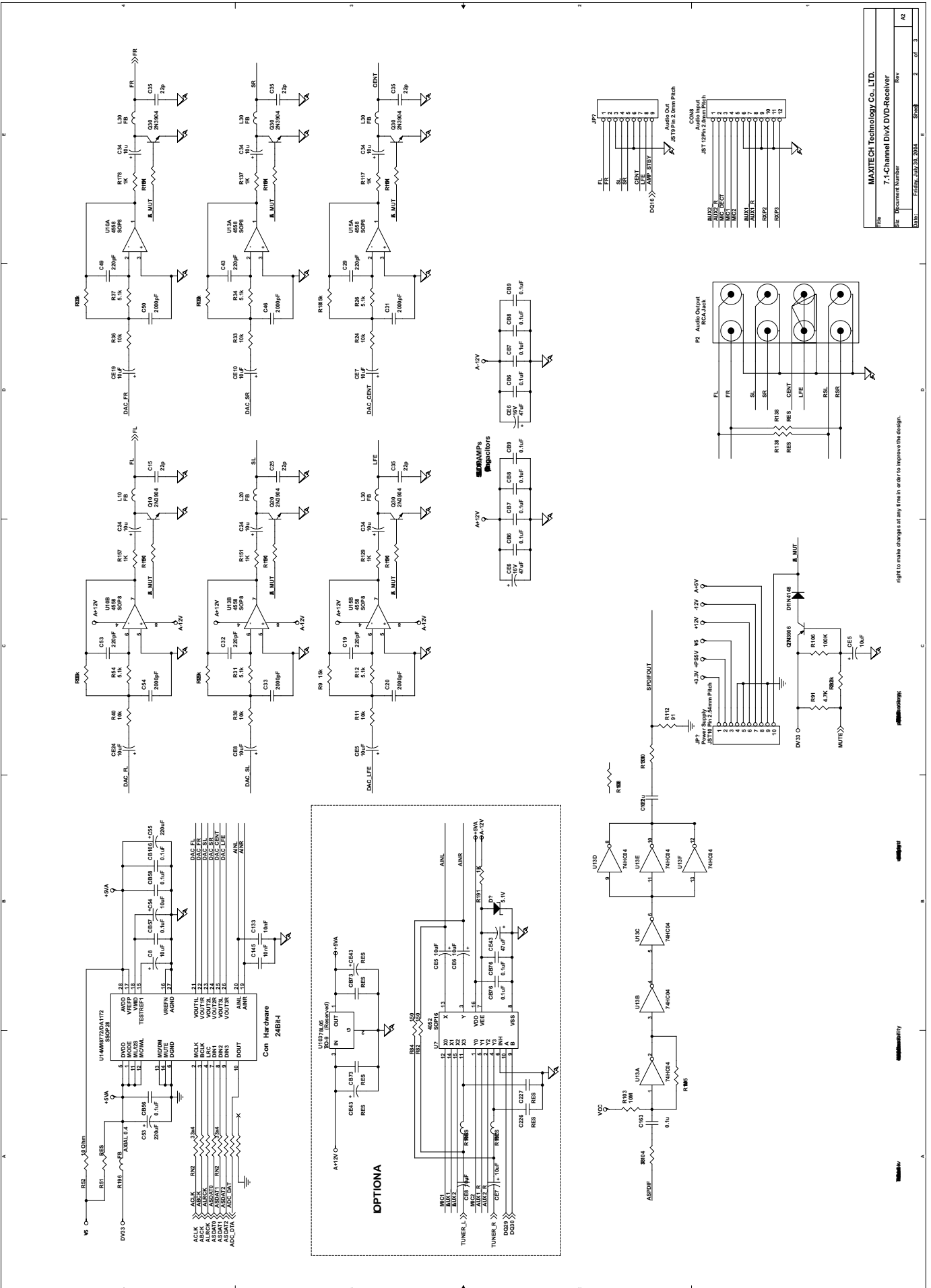
This board implements the back-end circuitry of a DVD player. It is composed of the following subsystems:

- * Microcontroller which does main control to all other sub-blocks of the system including user interface, driver interface, audio/video output.
- * Vaddis A/V Decoder IC decodes the bitstream coming from the DVD front-end drive, and optionally performs audio and video effects.
- * Audio Codec



MAXTECH Technology Co., Ltd.
 Maxtech DVD-Receiver MT1379 Solution
 Document Number: Rev 1.0
 Website: www.maxtech.com.tw

Please refer to the design.

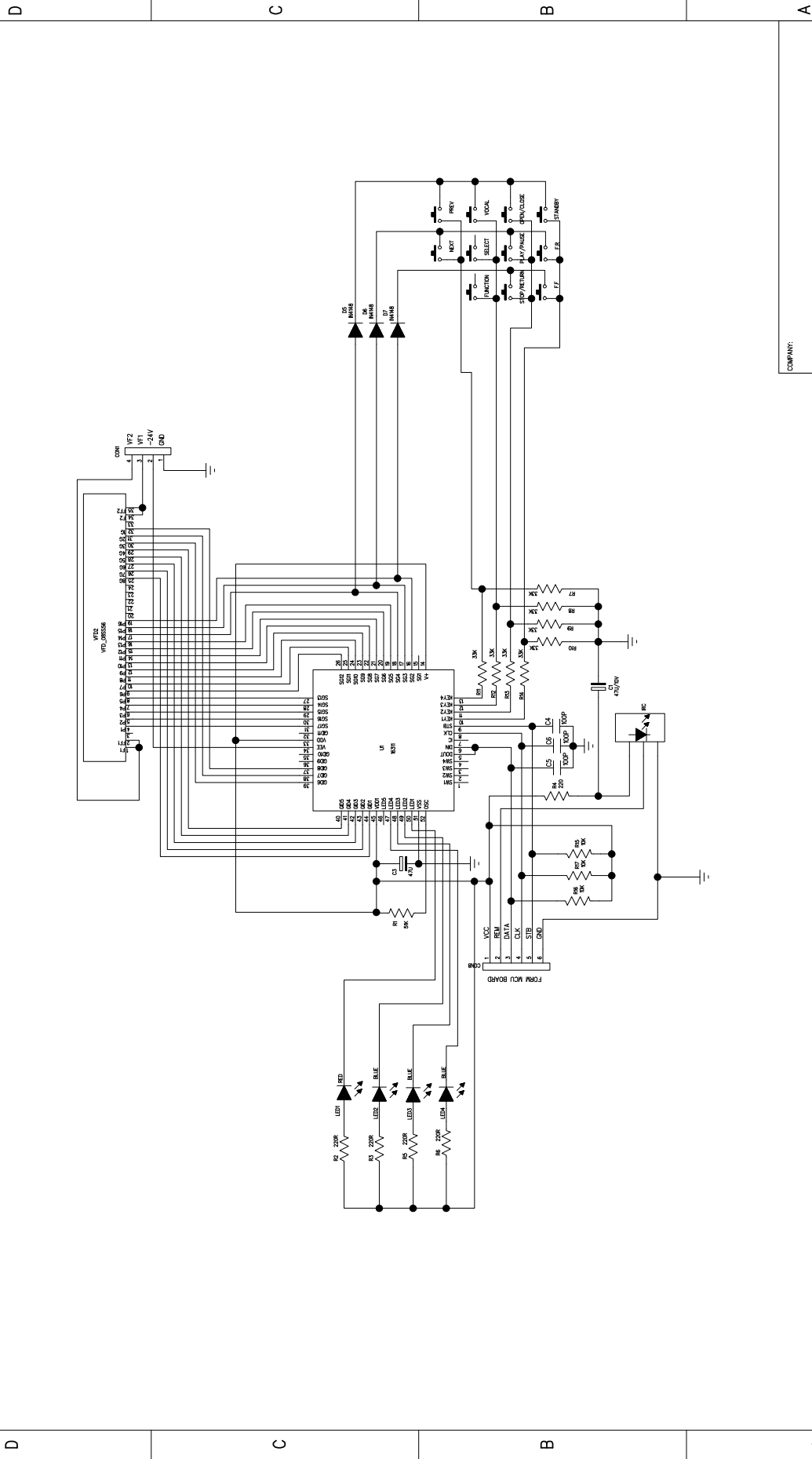


right to make changes at any time in order to improve the design.

REV	MAXTECH Technology Co., LTD.
REV	7-1-Channel DVD-Receiver
REV	Document Number
REV	Rev
REV	2
REV	OF 3
REV	DATE: 2000.07.20

1 2 3 4 5 6

REVISION RECORD		
LTR	ECO NO.	APPROVED DATE



DRAWN		DATED:	
CHECKED:		DATED:	
QUALITY CONTROL:		DATED:	
RELEASED:		DATED:	
COMPANY:	TITLE:	CODE:	SIZE:
DRAWING NO.:		REV.:	
SCALE:	SHEET:	OF:	

4.2.1 Front Panel Interface

6 Pin, Data Connector Pin Assignments

PIN	NAME	I/O	DESCRIPTION
1	DATA	I	IR sensor interrupt
2	CLK	O	Front Panel chip select
3	STB	O	Front Panel clock
4	GND	O	Front Panel Data output
5	VCC		
6	REM	I	Front Panel Data input

3Pin, Power Connector Pin Assignments

PIN	NAME	FROM	DESCRIPTION
1	VFD 1	SMPS	Segment and grid Voltage of the VFD
2	VFD 2	SMPS	Provide a DC supply to the cathode. To overcome the voltage difference between one and the other of the cathode.
3	-21V	SMPS	

There are 3 different devices operated by the PT6311 and S0791GC (Optional):

- * Vacuum Fluorescent Display (VFD)
- * Push-buttons
- * VFDs

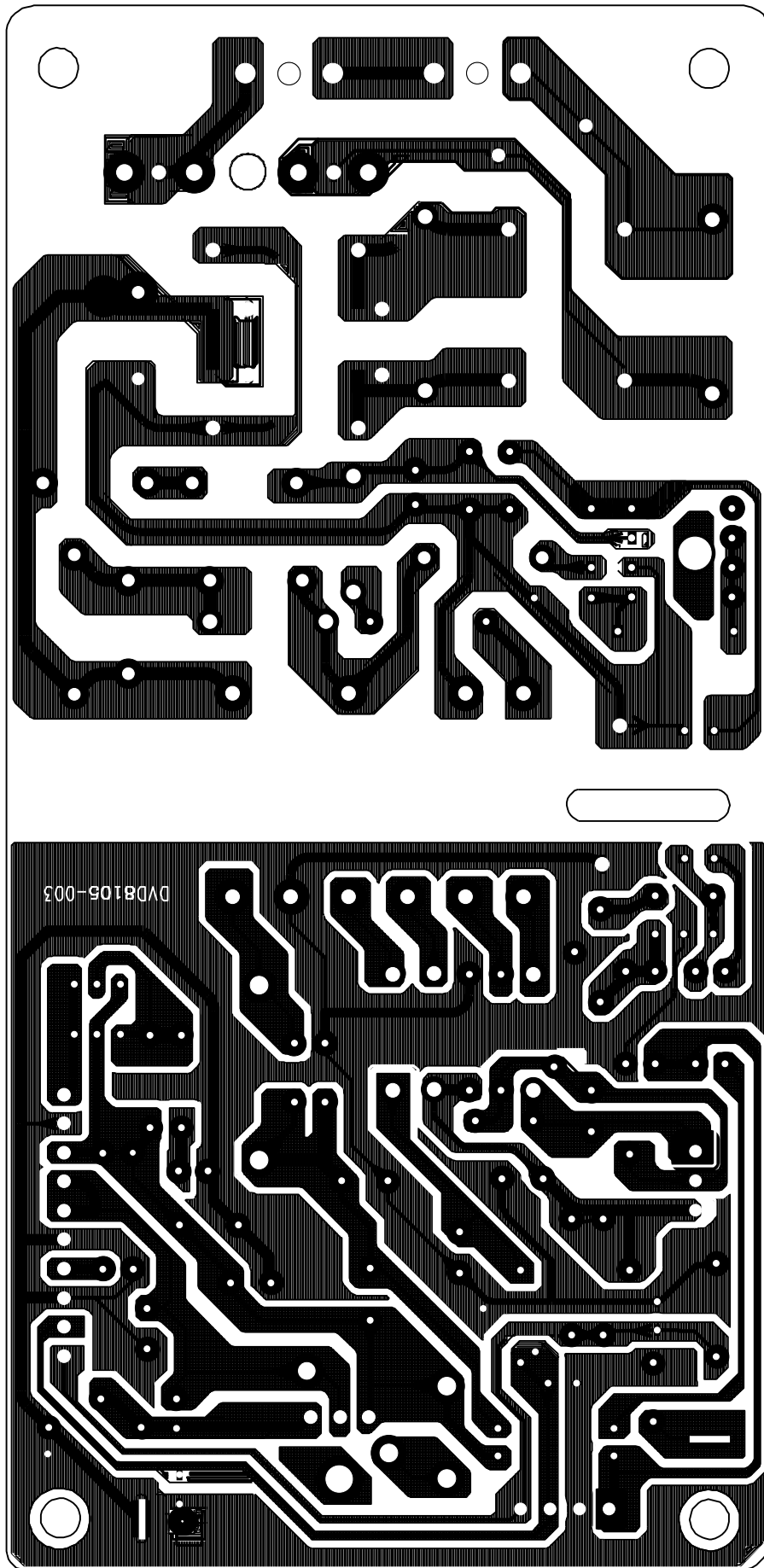
There is an option for a tray lamp and a joystick which is not currently assembled. The VFD display is custom made, implemented in a 6 grids by 16 segment matrix.

The VFD needs special voltage supply for operation:

- * V_{kk} which is -21V needed to drive the segments and grids of the VFD.
- * V_{f1}, V_{f2} which powers the electron cloud filament (cathode) with a differential voltage of 3.5V. This is a floating voltage difference generated by the power supply, and is biased to -21V in the front panel board by a Zener circuit from the -21V (V_{kk}) supply. Moving the bias towards a more positive number will reduce the segment brightness. V_{f1} & V_{f2} provide a DC supply to the cathode. To overcome the voltage difference between one end and the other of the cathode, it is geometrically tilted so that the segments observe the same potential and have all the same brightness. Other way to overcome the problem is to employ an AC supply to power the V_{f1} and V_{f2}.

4.3 SMPS

The mains power(220VAC) fed from K1 is filtered through 3C1, 3L1, 3C2 then rectified by D1, D2, D3 and D4 and generates an output at 300VDC. This 300VDC fed to 3TR1 (pin1, pin5) which connects to 5M02659R(pin3), then 5M02659R will automatically generate a 50KHz square waveform, this 50KHz square waveform controls the ON/OFF between 5M02659R pin1 and the ground. In normal condition, T1 primary (between pin2 and pin4) will create a 50KHz square waveform which is controlled by 5M02659R, this signal then fed to 3TR1 and generates 2 different potential voltages of 12V and 5V. The 12VDC and 5VDC then rectified by 3D11 and then filtered by 3L2, 3R9, 3C18, 3CC25 and 3C11. The feedback voltage is controlled by IC3 TL431 and IC2 PC817. When the output voltage is higher than 5V, the voltage at TL431(2.5V) is compared with R10 and send out a signal to 5M02659R, the output square waveform then will change to adjust the output voltage, this acts as a voltage stabilizer.



4.4.1 Adopt small lens: can adopt SONY310 .Hittachi .Mipseumi . Thomson act lens

4.5 Electric specification

4.5.1 Drive cell:adopt LD-300C-12400 electricity machine

5.2 Electricity machine work voltage is 3V-5.9V

5.3 General work voltage is 3.3V-5V

5.4 Unilateralism(com or go) move time:<1.5S(add 5V voltage)

5.5 In 5 °C-10°C work current is <120mA

4.6 Testing condition

6.1 Position: level placed

6.2 environment: temperature 22 ± 2 °C

Humidity $50 \pm 5\%$

6.3 Turnover storehouse voltage: $5V \pm 0.5V$

• 6.4 Standard DVD lens testing frock

6.5 Standard DVD testing dish



5. DESCRIPTION OF THE INTEGRATED CIRCUITS

5.1 SMPS TRANSFORMER

1. GENERAL INFORMATION

Main Voltage Operations:	90Vac - 265 Vac
Main Drop-out Voltage:	Max. 90 Vac
Mains Start-up Voltage:	Max. 90 Vac
Operating Frequency:	60 KHz

2. ELECTRICAL CHARACTERISTICS

2.1 STATIC CHARACTERISTICS

WINDING	PIN.NO	INDUCTANCE	DESCRIPTION
Primary Inductance	2-4	1.5mH10%	<0.50W

1. Primary Leakage inductance (Pin 2-4) L1.5mH

2.2 WITHSTANDING VOLTAGE

The transformer shall withstand a voltage of 4 Kvms for 1 minute and 1 mA between primary and secondary winding and also 2 Kvms for 1 minute and 1 mA between primary winding with core and secondary winding with core.

2.3 INSULATION RESISTANCE

The insulation resistance shall be more than 500M between primary and secondary windings when the applied voltage 300 Vdc for 1 minute

2.4 ELECTRICAL CHARACTERISTICS

1. Before taking measurement Pp01 will be to give 5.0Vdc on 5.0Vdc line at Minimum setting of controls and a mains voltage 220 Vac.
2. Before taking a measurement, DVD set should be working at least 5 minutes on Normal condition

5.2 FRONT PANEL DRIVER IC FOR VIR (PT6311)

5.2.1 General Description

VFD Driver/Controller IC

PT6311

BLOCK DIAGRAM

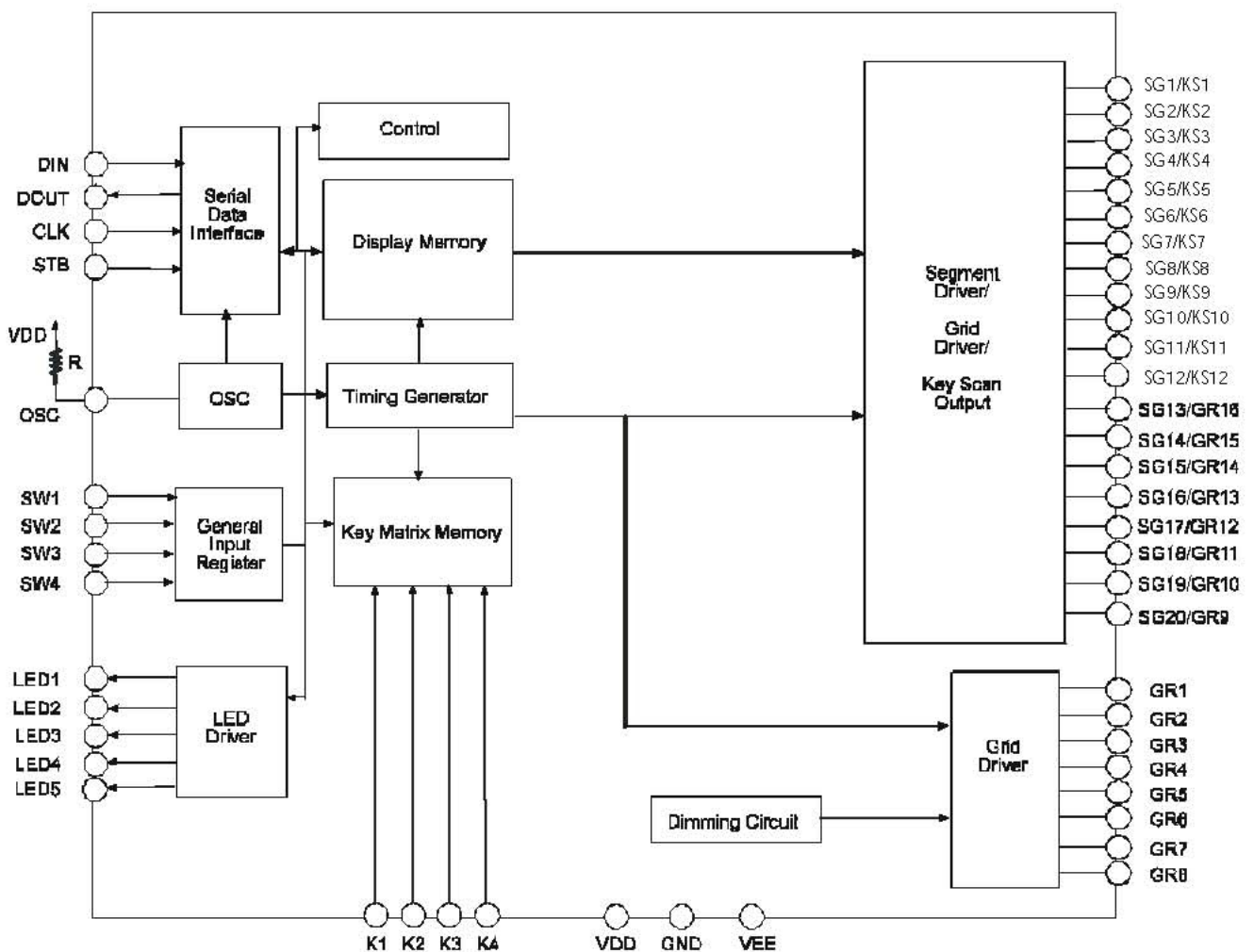


Figure 1: PT6311 Internal Block Diagram

PIN CONFIGURATION

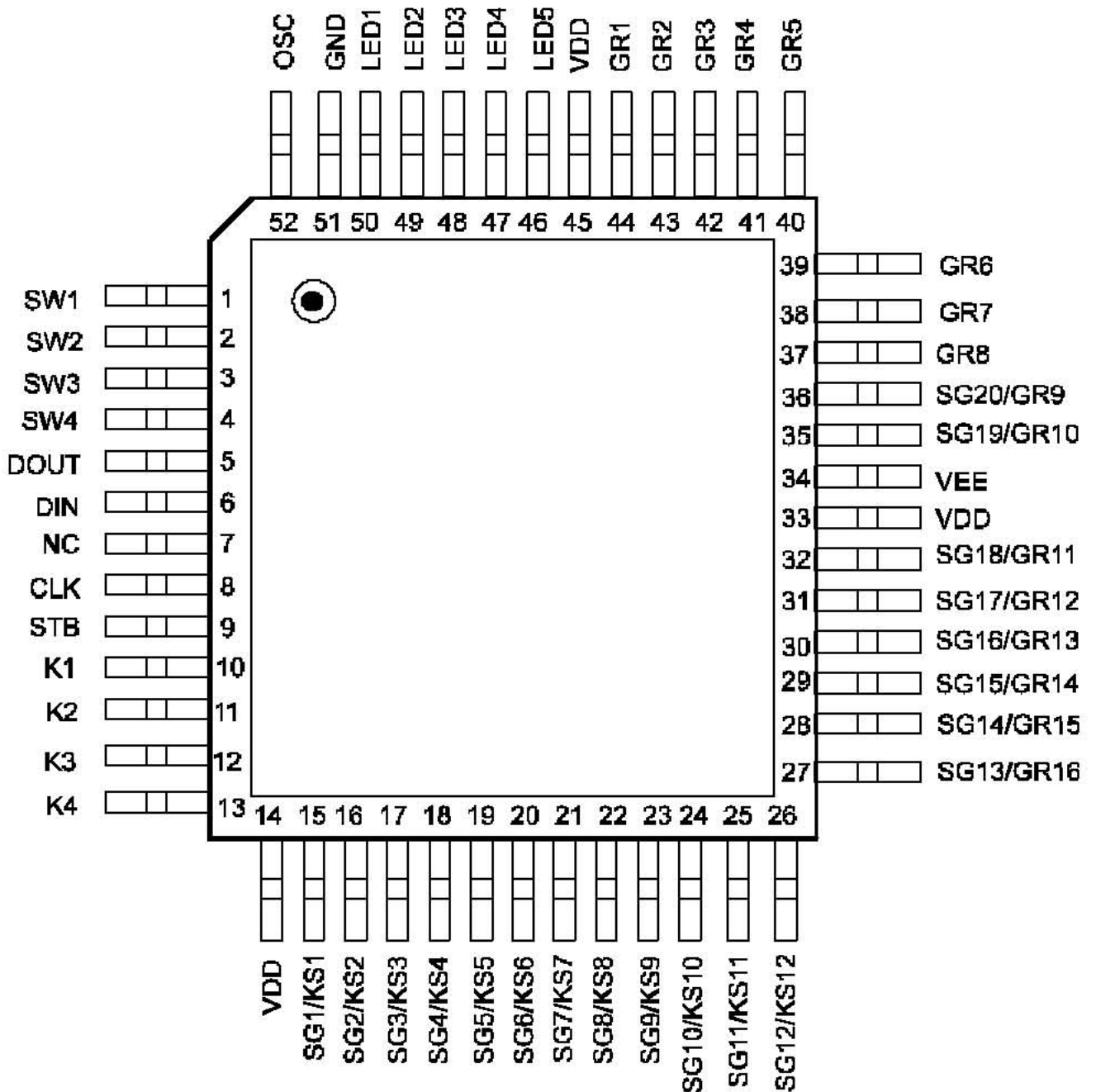


Figure 2: PT6311 Pin Configuration

PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SW 1 to SW 4	I	General Purpose Input Pins	1 to 4
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	5
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	6
NC	-	No Connection	7
CLK	I	C lock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	8
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.	9
K1 to K4	I	Key Data Input Pins The data inputted to these pins are latched at the end of the display cycle.	10 to 13
VDD	-	Logic Power Supply	14, 33, 45
SG1/KS1 to SG12/KS12	O	High-Voltage Segment Output Pins Also acts as the Key Source	15 to 26
SG20/GR9 to SG19/GR10 SG18/GR11 to SG13/GR16	O	High Voltage Segment/Grid Output Pins	36 to 35 32 to 27
VEE	-	Pull-Down Level	34
GR1 to GR8	O	High-Voltage Grid Output Pins	44 to 37
LED1 to LED5	O	LED Output Pin	50 to 46
GND	-	Ground Pin	51
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	52

12-GRID X 16-SEGMENT VFD APPLICATION CIRCUIT

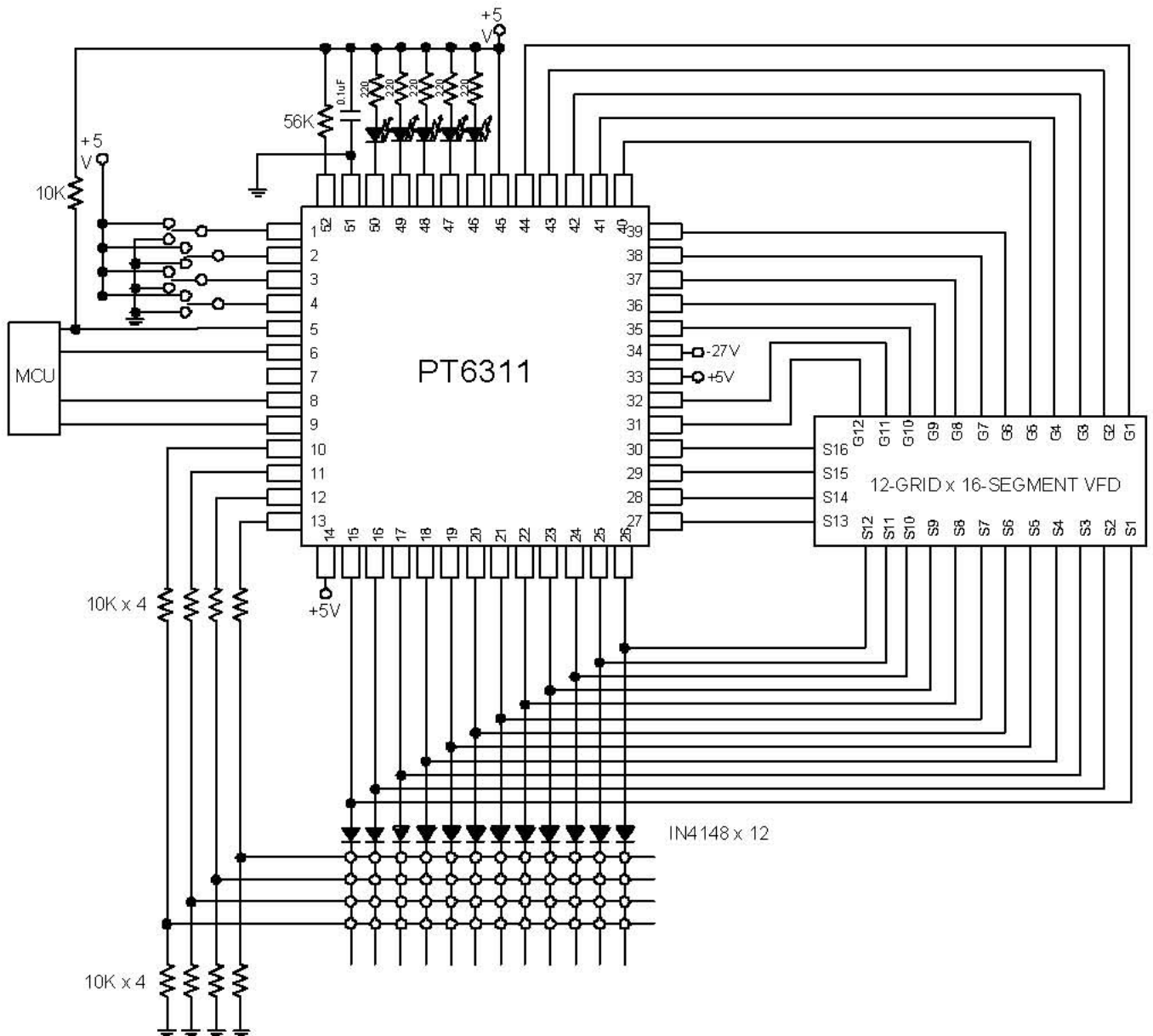


Figure 18: PT6311 Application Circuit

5.3 SWPS CONTROLLER IC (5M02659)



www.fairchildsemi.com

KA5x02xx-SERIES

**KA5H0265RC, KA5M0265R, KA5L0265R,
KA5H02659RN/KA5M02659RN, KA5H0280R,
KA5M0280R**

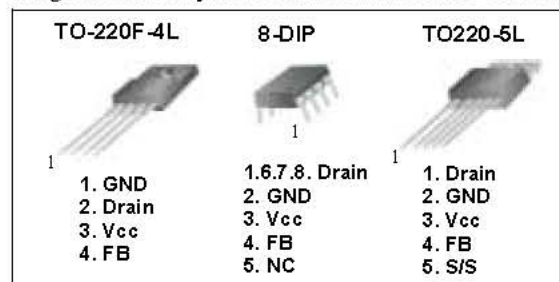
Fairchild Power Switch(FPS)

Features

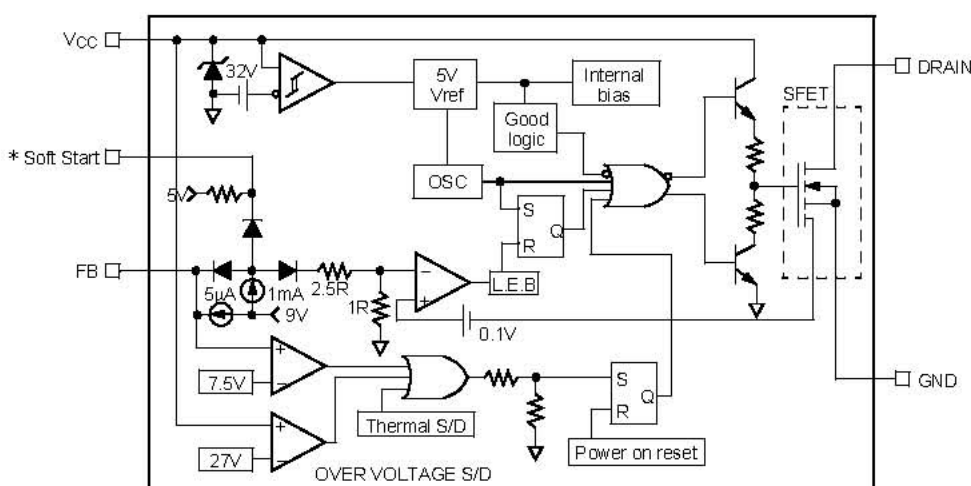
- Precision Fixed Operating Frequency (100/67/50kHz)
- Low Start-up Current (Typ. 100uA)
- Pulse by Pulse Current Limiting
- Over Load Protection
- Over Voltage Protection (Min. 25V)
- Internal Thermal Shutdown Function
- Under Voltage Lockout
- Internal High Voltage Sense FET
- Auto-Restart Mode

Description

The Fairchild Power Switch(FPS) product family is specially designed for an off-line SMPS with minimal external components. The Fairchild Power Switch(FPS) consist of high voltage power SenseFET and current mode PWM IC. Included PWM controller features integrated fixed oscillator, under voltage lock out, leading edge blanking, optimized gate turn-on/turn-off driver, thermal shut down protection, over voltage protection, and temperature compensated precision current sources for loop compensation and fault protection circuitry-compared to discrete MOSFET and controller or R_{OC} switching converter solution. The Fairchild Power Switch(FPS) can reduce total component count, design size, weight and at the same time increase efficiency, productivity, and system reliability. It has a basic platform well suited for cost-effective design in either a flyback converter or a forward converter.



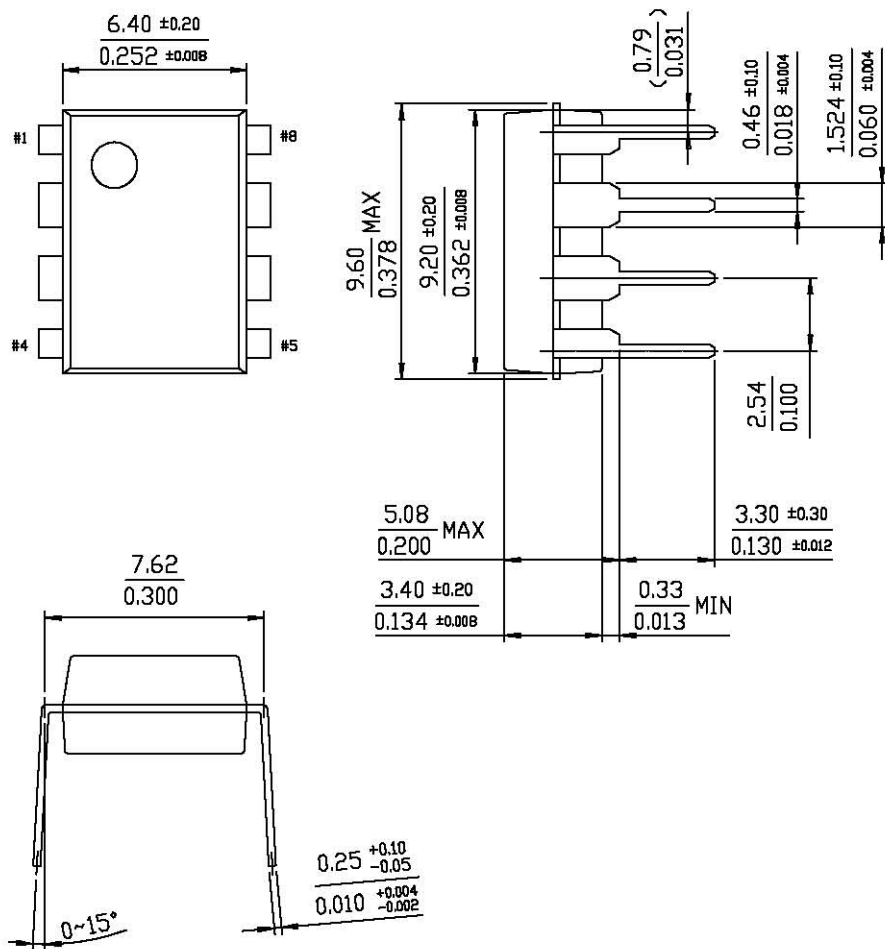
Internal Block Diagram



* KA5H0265RC

Package Dimensions (Continued)

8-DIP



Electrical Characteristics (SFET Part)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
KA5x0265xRx						
Drain-Source Breakdown Voltage	BVDSS	VGS=0V, ID=50μA	650	-	-	V
Zero Gate Voltage Drain Current	IDSS	VDS=Max. Rating, VGS=0V	-	-	50	μA
		VDS=0.8Max. Rating, VGS=0V, TC=125°C	-	-	200	μA
Static Drain-Source on Resistance ^(Note)	RDS(ON)	VGS=10V, ID=0.5A	-	5.0	6.0	Ω
Forward Transconductance ^(Note)	gfs	VDS=50V, ID=0.5A	1.5	2.5	-	S
Input Capacitance	Ciss	VGS=0V, VDS=25V, f=1MHz	-	550	-	pF
Output Capacitance	Coss		-	38	-	
Reverse Transfer Capacitance	Crss		-	17	-	
Turn on Delay Time	td(on)	VDD=0.5B VDSS, ID=1.0A (MOSFET switching time is essentially independent of operating temperature)	-	20	-	nS
Rise Time	tr		-	15	-	
Turn Off Delay Time	td(off)		-	55	-	
Fall Time	tf		-	25	-	
Total Gate Charge (Gate-Source+Gate-Drain)	Qg	VGS=10V, ID=1.0A, VDS=0.5B VDSS (MOSFET switching time is essentially independent of operating temperature)	-	-	35	nC
Gate-Source Charge	Qgs		-	3	-	
Gate-Drain (Miller) Charge	Qgd		-	12	-	
KA5x0280R						
Drain-Source Breakdown Voltage	BVDSS	VGS=0V, ID=50μA	800	-	-	V
Zero Gate Voltage Drain Current	IDSS	VDS=Max. Rating, VGS=0V	-	-	50	μA
		VDS=0.8Max. Rating, VGS=0V, TC=125°C	-	-	200	μA
Static Drain-Source on Resistance ^(Note)	RDS(ON)	VGS=10V, ID=0.5A	-	5.6	7.0	Ω
Forward Transconductance ^(Note)	gfs	VDS=50V, ID=0.5A	1.5	2.5	-	S
Input Capacitance	Ciss	VGS=0V, VDS=25V, f=1MHz	-	250	-	pF
Output Capacitance	Coss		-	52	-	
Reverse Transfer Capacitance	Crss		-	25	-	
Turn on Delay Time	td(on)	VDD=0.5B VDSS, ID=1.0A (MOSFET switching time is essentially independent of operating temperature)	-	21	-	nS
Rise Time	tr		-	28	-	
Turn Off Delay Time	td(off)		-	77	-	
Fall Time	tf		-	24	-	
Total Gate Charge (Gate-Source+Gate-Drain)	Qg	VGS=10V, ID=1.0A, VDS=0.5B VDSS (MOSFET switching time is essentially independent of operating temperature)	-	-	60	nC
Gate-Source Charge	Qgs		-	15	-	
Gate-Drain (Miller) Charge	Qgd		-	20	-	

Note:

1. Pulse test: Pulse width ≤ 300μS, duty cycle ≤ 2%

2. $S = \frac{1}{R}$

KA5X02XX-SERIES
Electrical Characteristics (Control Part) (Continued)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
UVLO SECTION						
Start Threshold Voltage	VSTART	VFB=GND	14	15	16	V
Stop Threshold Voltage	VSTOP	VFB=GND	8.2	8.8	9.4	V
OSCILLATOR SECTION						
Initial Accuracy	FOSC	KA5H0265xRx KA5H0280R	90	100	110	kHz
Initial Accuracy	FOSC	KA5M0265xRx KA5M0280R	61	67	73	kHz
Initial Accuracy	FOSC	KA5L0265R	45	50	55	kHz
Frequency Change With Temperature ⁽²⁾	$\Delta F/\Delta T$	-25°C ≤ Ta ≤ +85°C	-	±5	±10	%
Maximum Duty Cycle	Dmax	KA5H0265xRx KA5H0280R	62	67	72	%
Maximum Duty Cycle	Dmax	KA5M0265xRx KA5M0280R KA5L0265R	72	77	82	%
FEEDBACK SECTION						
Feedback Source Current	IFB	Ta=25°C, 0V ≤ Vfb ≤ 3V	0.7	0.9	1.1	mA
Shutdown Feedback Voltage	VSD	Vfb ≤ 6.5V	6.9	7.5	8.1	V
Shutdown Delay Current	I _{delay}	Ta=25°C, 5V ≤ Vfb ≤ VSD	4	5	6	μA
SOFT START SECTION						
Soft Start Voltage	VSS	KA5H0265RC	4.7	5.0	5.3	V
Soft Start Current	ISS		0.8	1.0	1.2	mA
REFERENCE SECTION						
Output Voltage ⁽¹⁾	Vref	Ta=25°C	4.80	5.00	5.20	V
Temperature Stability ⁽¹⁾⁽²⁾	Vref/ΔT	-25°C ≤ Ta ≤ +85°C	-	0.3	0.6	mV/°C
CURRENT LIMIT(SELF-PROTECTION)SECTION						
Peak Current Limit	I _{OVER}	KA5x02659RN	0.79	0.9	1.01	A
Peak Current Limit	I _{OVER}	KA5x0265Rx KA5x0280R	1.05	1.2	1.34	A
PROTECTION SECTION						
Over Voltage Protection	VOVP	VCC ≥ 24V	25	27	29	V
Thermal Shutdown Temperature ⁽¹⁾	TSD	-	140	160	-	°C
TOTAL DEVICE SECTION						
Start-up Current	ISTART	VCC=14V	-	100	170	μA
Operating Supply Current (Control Part Only)	IOPR	VCC ≤ 28	-	7	12	mA

Note:

1. These parameters, although guaranteed, are not 100% tested in production
2. These parameters, although guaranteed, are tested in EDS (wafer test) process

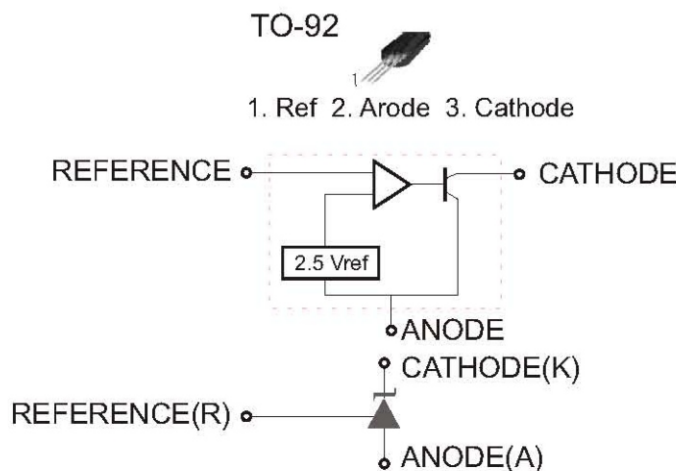
5.4 SMPS PROGRAMMABLE SHUNT REGULATOR (FAIRCHILD TL 431)

Features

- * Programmable output voltage to 36volts
- * Low dynamic output impedance 0.20 typical
- * Sink current capability of 1.0 to 100mA
- * Equivalent full-range temperature coefficient of 50 ppm °C typical
- * Temperature compensated for operation over full rated operating temperature range
- * Low output noise voltage
- * Fast turn-on response

Description

The TL 431/TL 431A are three-terminal adjustable regulator series with a guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between VREF (approximately 2.5 volts) and 36 volts with two external resistors. These devices have a typical dynamic output impedance of 2.0W Active output circuitry provides a very sharp turn-on characteristic making these devices excellent replacement for zener diodes in many applications



Absolute maximum ratings

Parameter	Symbol	Value	Unit
Cathode voltage	VKA	37	V
Cathode current Range (Continuous)	IKA	-100 ~ +150	MA
Reference Input Current Range	IREF	0.05 ~ +10	MA
Power dissipation D,Z Suffix Package N Suffix Package	PD	770 1000	MW MW
Operating Temperature Range	TOPR	-25 ~ +85	°C
Storage Temperature Range	TSTG	-65 ~ +150	°C

Recommended Operating conditions

Parameter	Symbol	Value	Value	Value	Unit
Cathode voltage	VKA	VREF	-	36	V
Cathode Current	IKA	1.0	-	100	MA

5.5 LINE FILTER (2 X 60mH)

ELECTRICAL DATA

Inductance: L1-2=L3-4=30mH - 15% - +20%

Resistance: R 1-2 = R 3-4 = 1.5 ohm (max)

Rated current: I_{rms} = 0.50 A
(F= 1 KHz V= 1 Vms)

LEAKAGE INDUCTANCE

L 1-2 = L 3-4 100+/- 20%uH NOTES

CIRCUIT DIAGRAM

