AKAI

PORTABLE DVD

Models:
ADP-841
ADP-841M

SERVICE MANUAL

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Service Manual

1. The System Block Diagram & the Block's Function Description
2. Schematic Circuit Diagram
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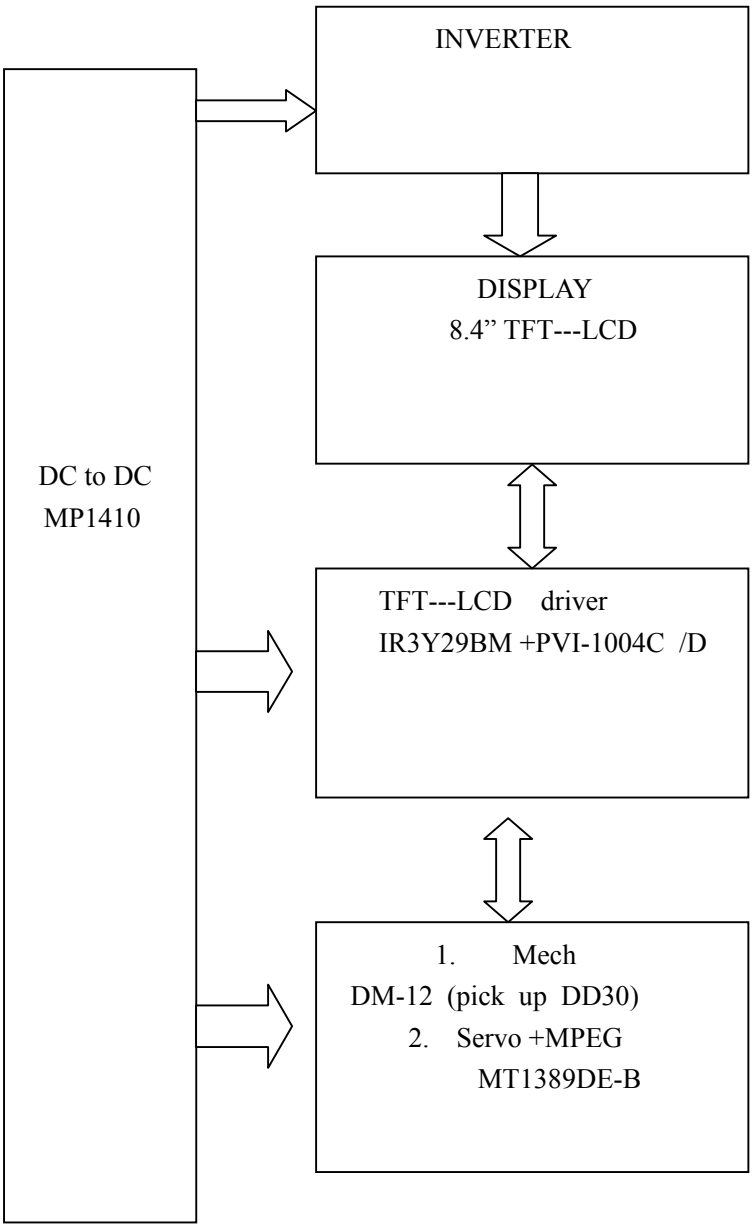
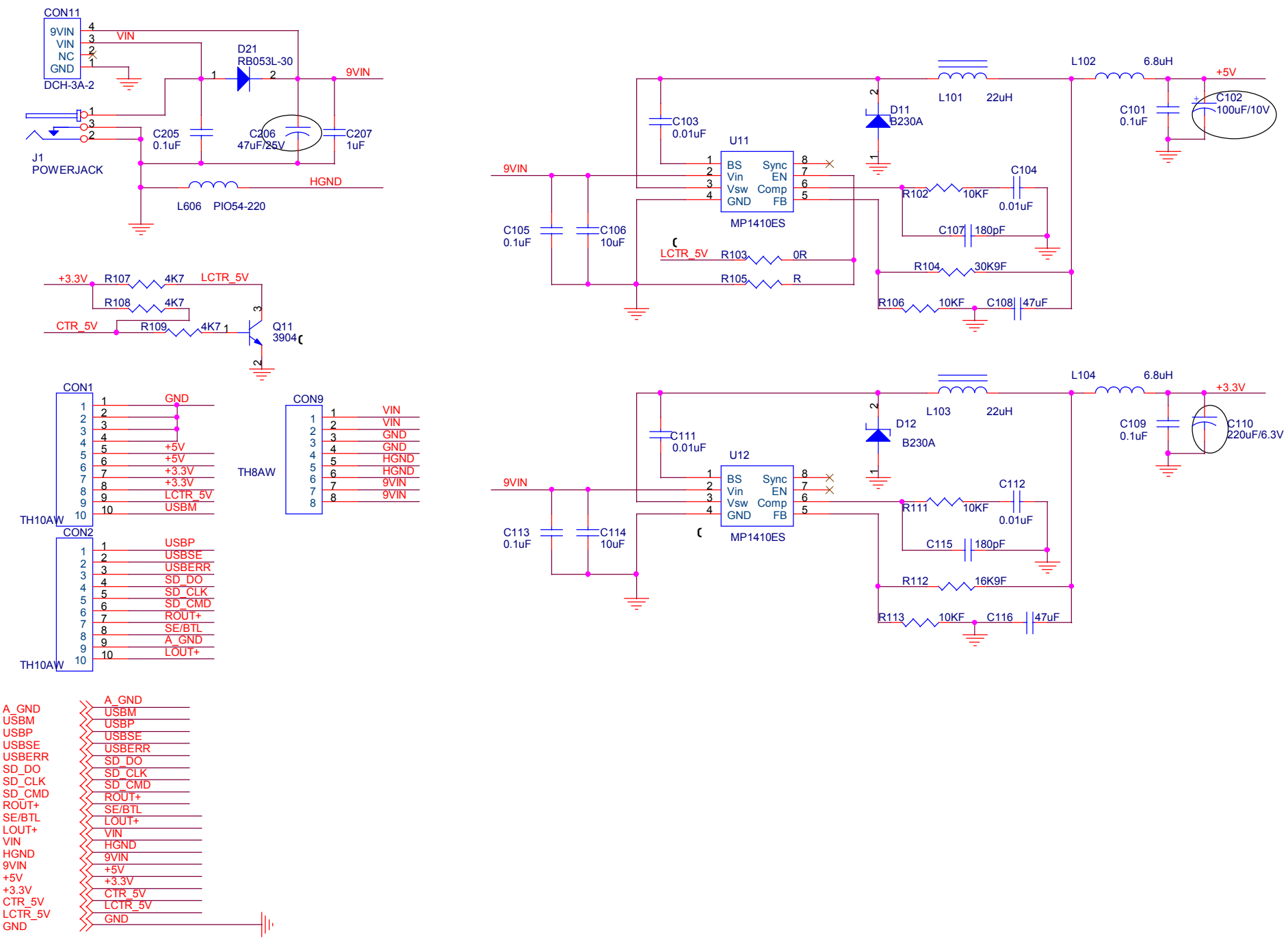
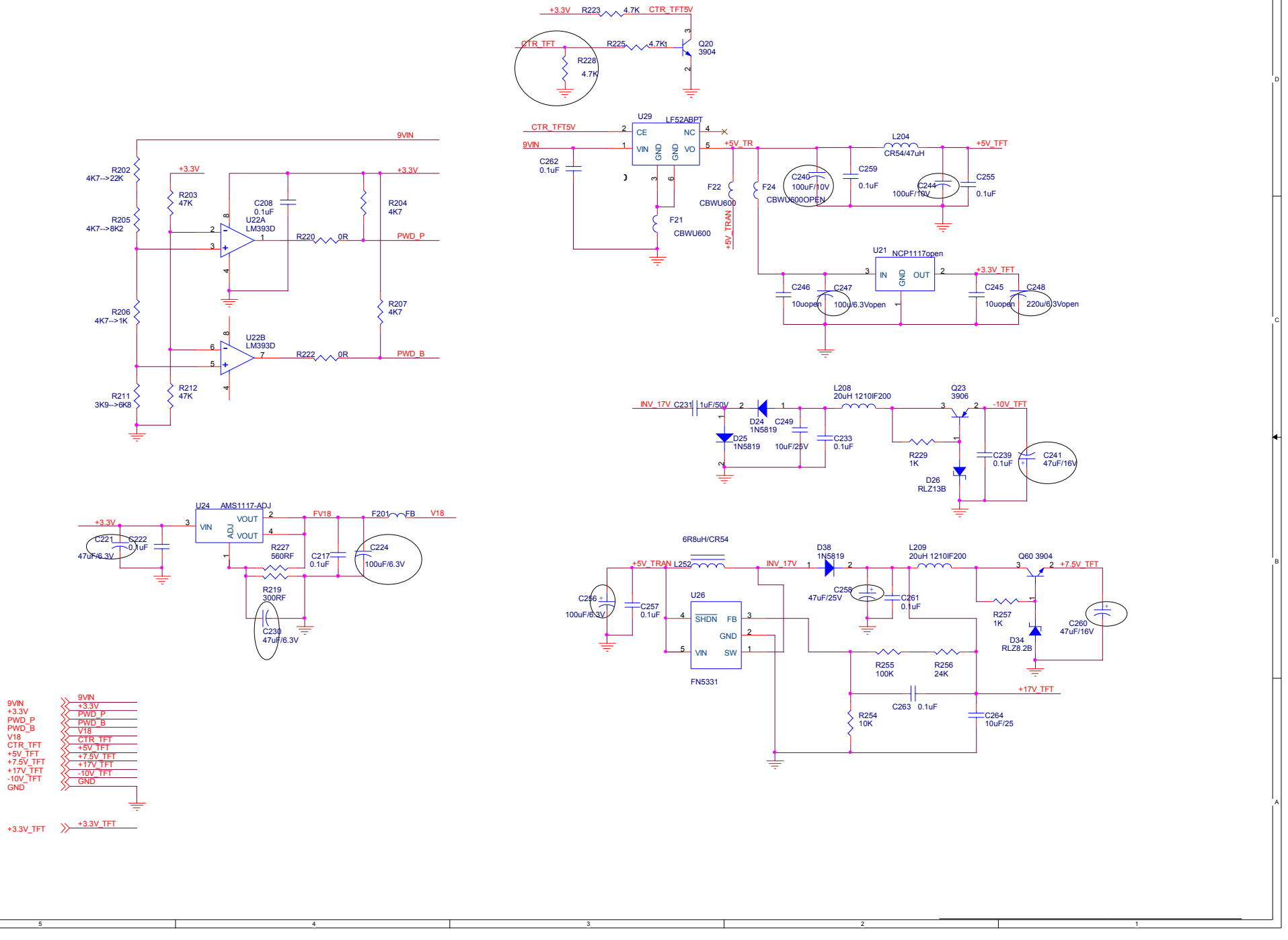
1. The System Block Diagram & the Block's Function Description

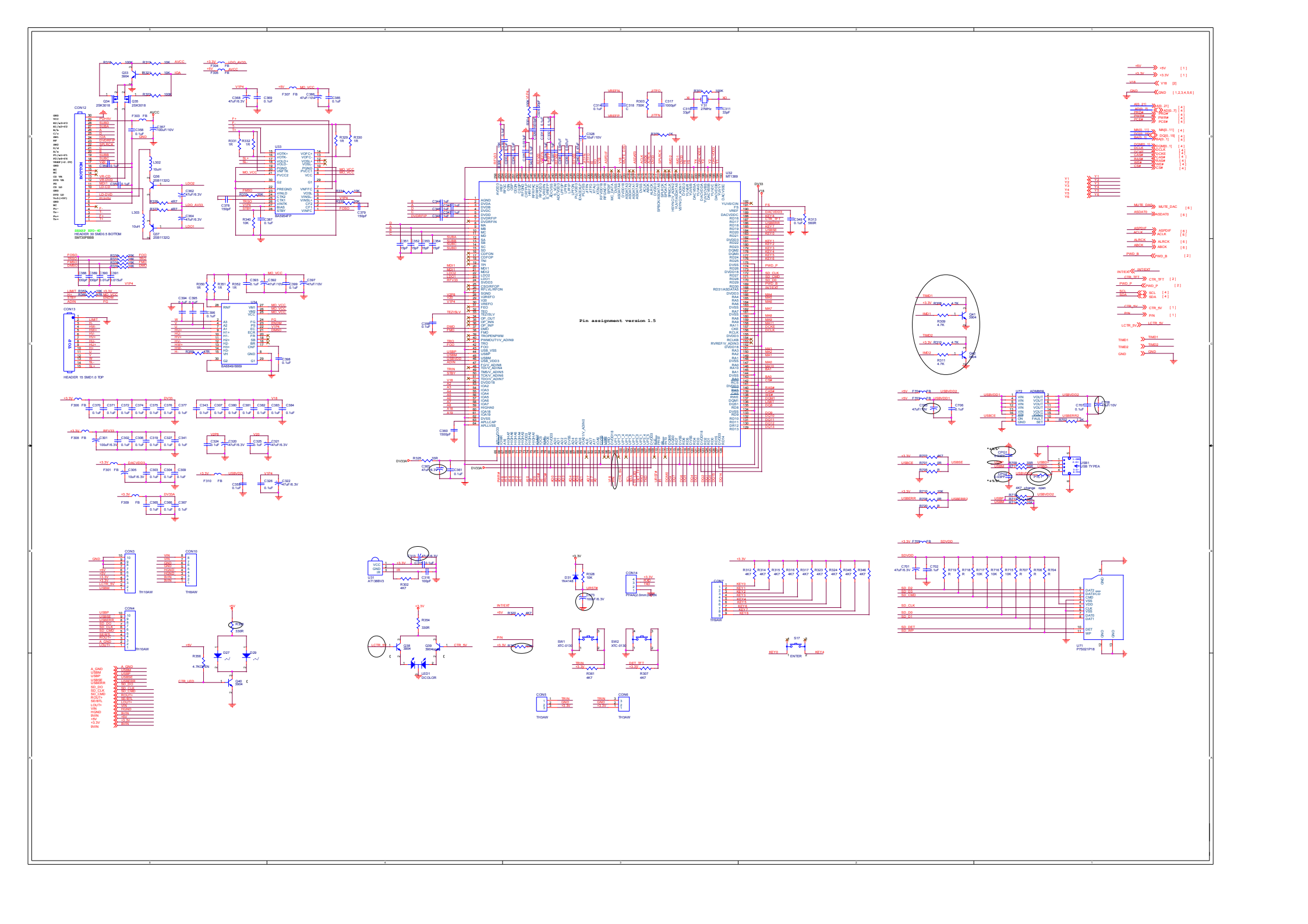
DVD System Block

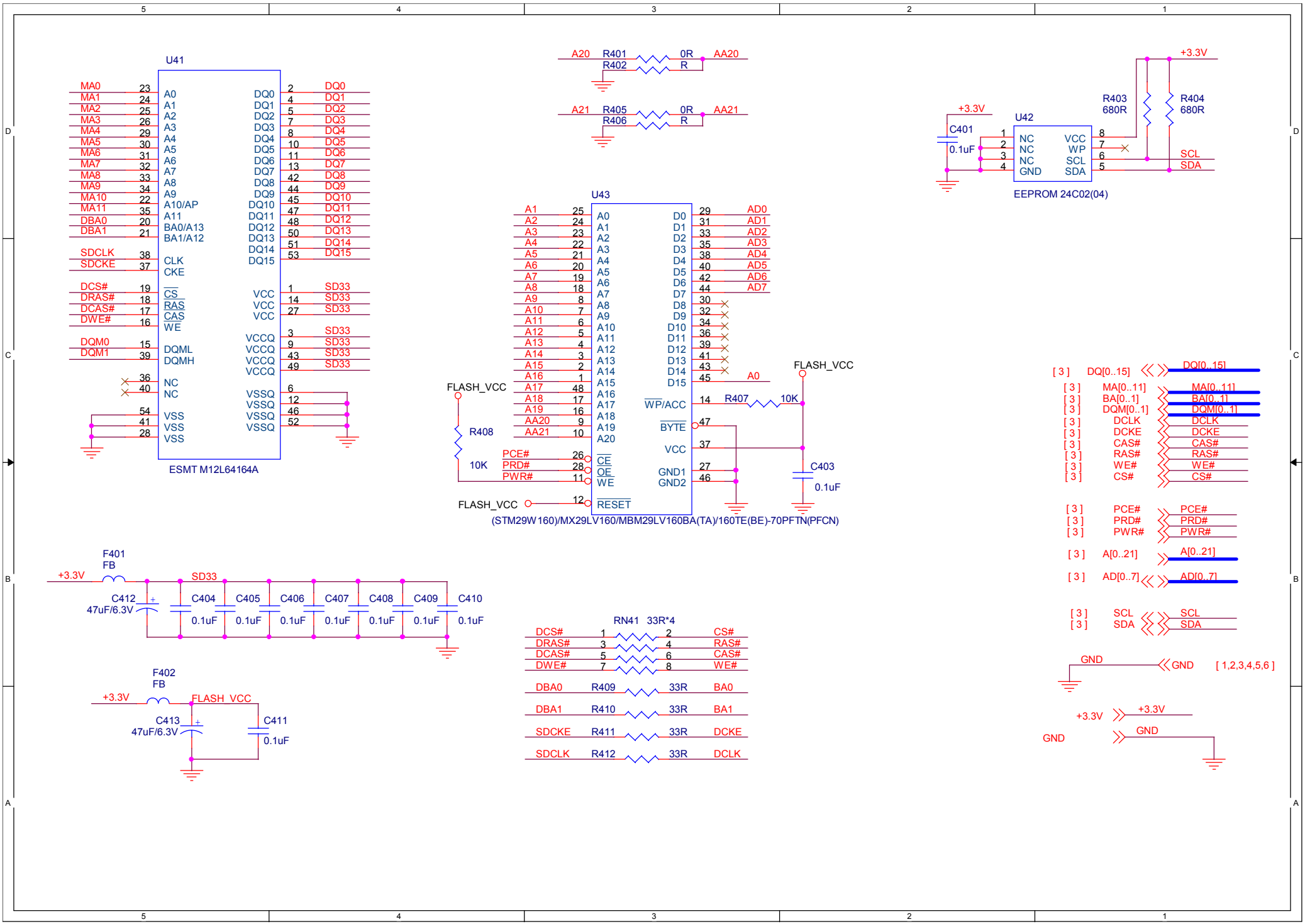


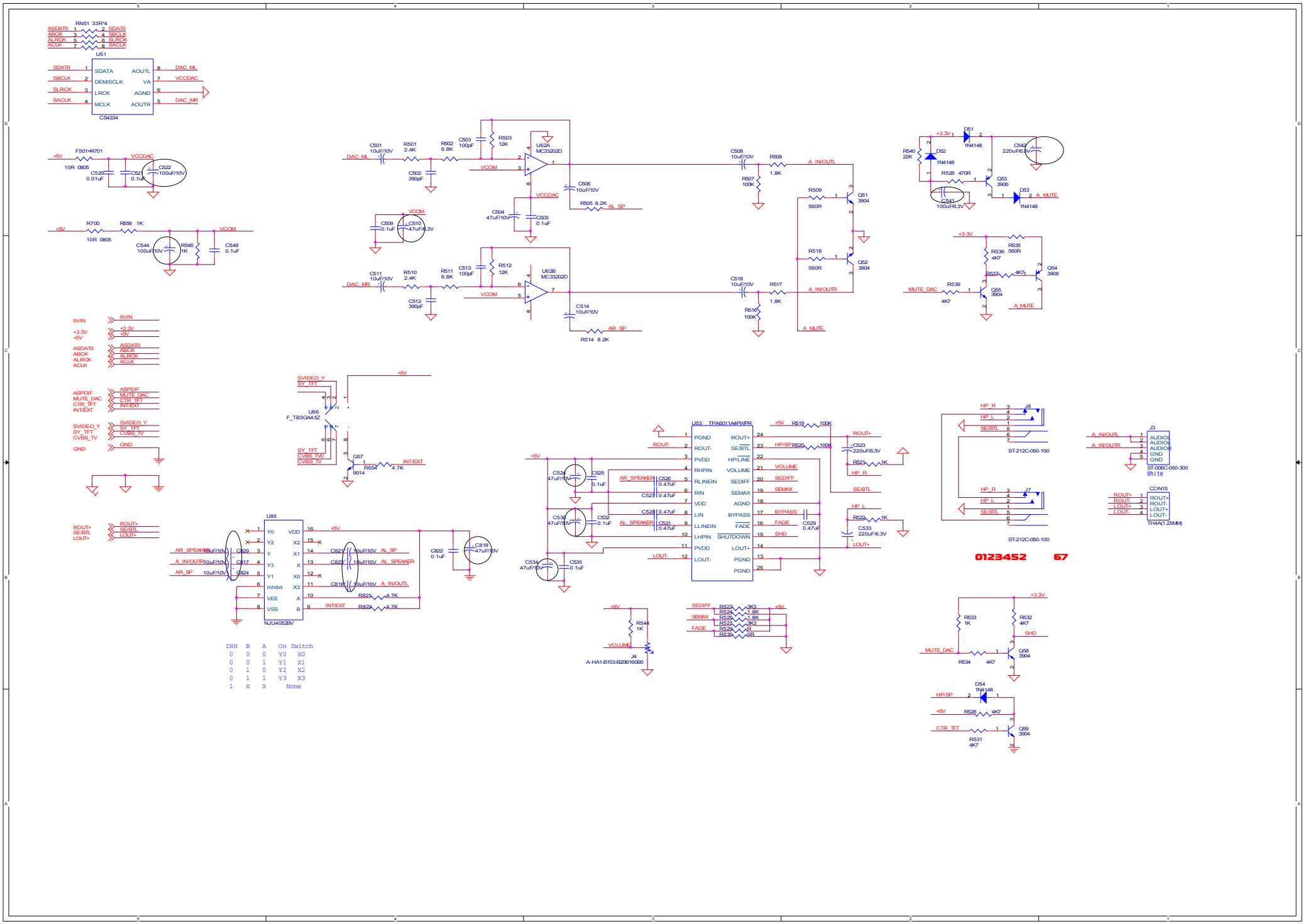
2. Schematic Circuit Diagram

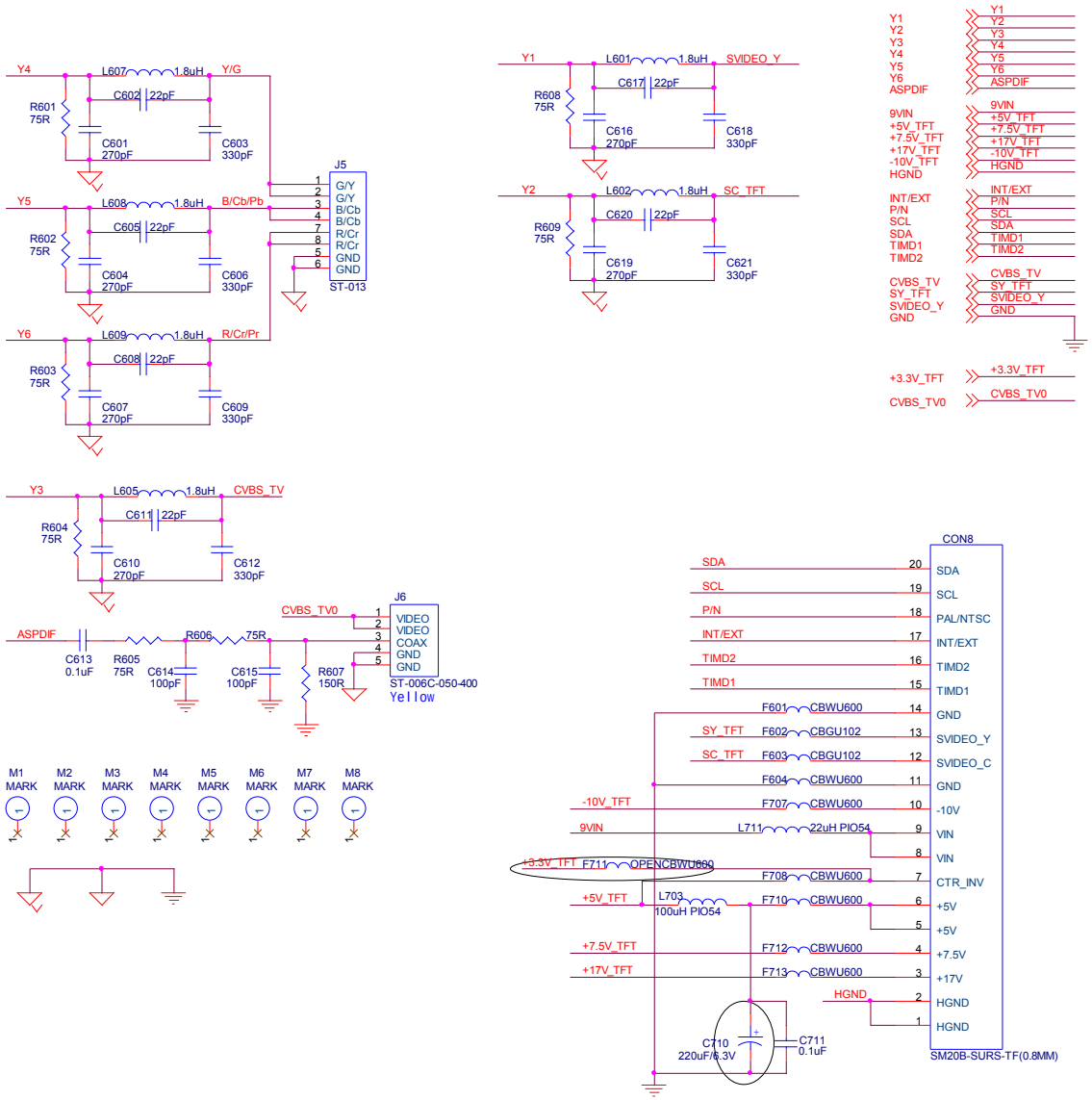

CON11
9VIN
VIN
NC
GND
DCH-3A-2
VIN
D21
RB053L-30
9VIN
J1
POWERJACK
C205
0.1uF
C206
47uF/25V
C207
1uF
HGND
L606 PIO54-220
+3.3V
R107 4K7
LCTR_5V
R108 4K7
CTR_5V
R109 4K7
Q11
3904
CON1
GND
+5V
+5V
+3.3V
+3.3V
LCTR_5V
USBM
TH10AW
CON9
VIN
VIN
GND
GND
HGND
HGND
9VIN
9VIN
TH8AW
CON2
USBP
USBSE
USBERR
SD_DO
SD_CLK
SD_CMD
ROUT+
SE/BTL
A_GND
LOUT+
TH10AW
A_GND
USBM
USBP
USBSE
USBERR
SD_DO
SD_CLK
SD_CMD
ROUT+
SE/BTL
LOUT+
VIN
HGND
9VIN
+5V
+3.3V
CTR_5V
LCTR_5V
GND
L101 22uH
L102 6.8uH
+5V
D11
B230A
C103
0.01uF
U11
BS Sync
Vin EN
Vsw Comp
GND FB
MP1410ES
9VIN
C105
0.1uF
C106
10uF
LCTR_5V
R103 0R
R105 R
C101
0.1uF
C102
100uF/10V
C104
0.01uF
R102 10KF
C107 180pF
R104 30K9F
R106 10KF
C108 47uF
L103 22uH
L104 6.8uH
+3.3V
D12
B230A
C111
0.01uF
U12
BS Sync
Vin EN
Vsw Comp
GND FB
MP1410ES
9VIN
C113
0.1uF
C114
10uF
C109
0.1uF
C110
220uF/6.3V
C112
0.01uF
R111 10KF
C115 180pF
R112 16K9F
R113 10KF
C116 47uF

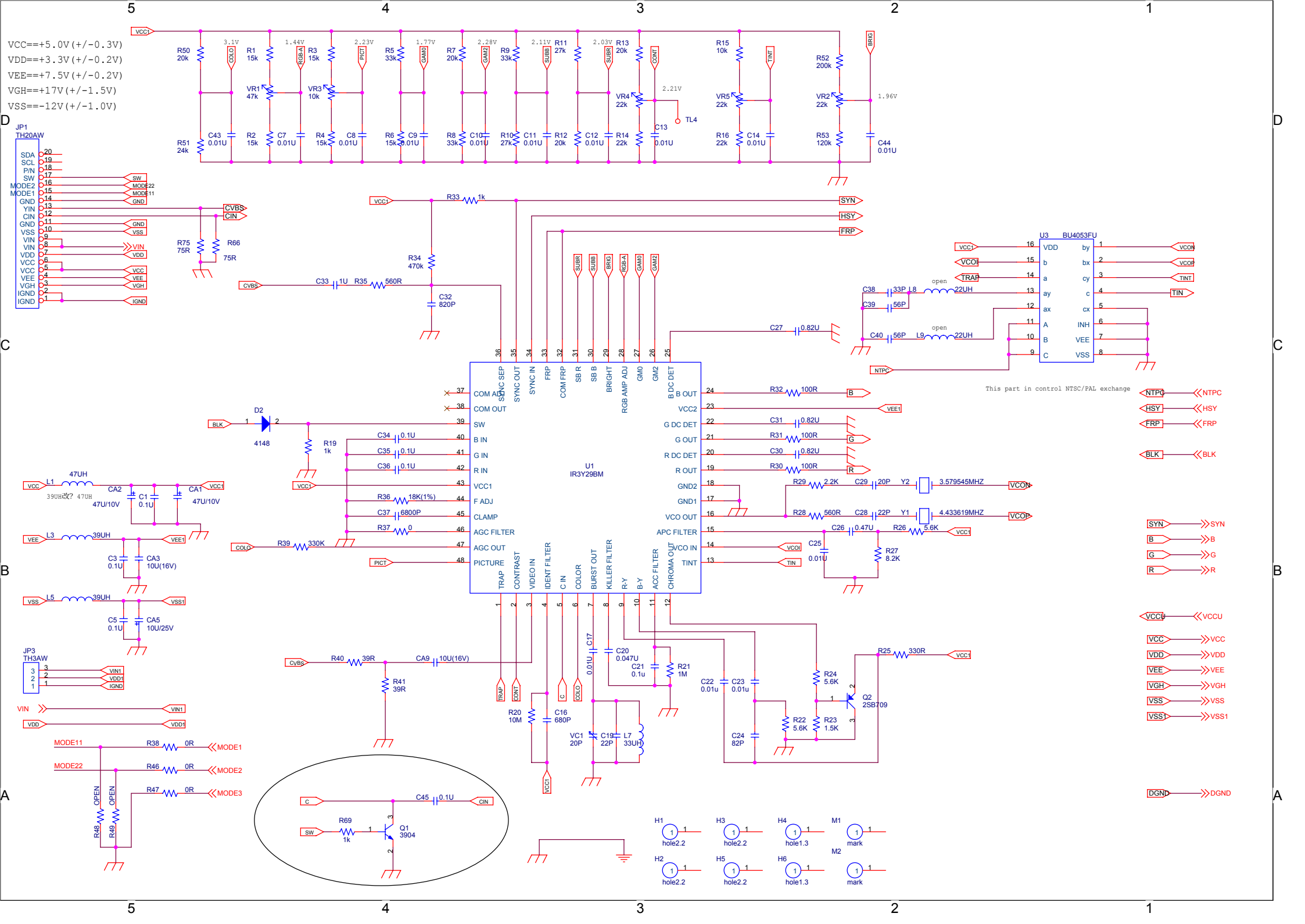

+3.3V R223 4.7K CTR_TFT5V
CTR_TFT R225 4.7K1 Q20 3904
R228 4.7K
9VIN
R202 4K7-->22K
R203 47K
R205 4K7-->8K2
R206 4K7-->1K
R211 3K9-->6K8
R212 47K
C208 0.1uF
U22A LM393D
U22B LM393D
R220 0R
R222 0R
R204 4K7
R207 4K7
PWD_P
PWD_B
U29 LF52ABPT
CTR_TFT5V
9VIN
C262 0.1uF
CE NC VIN GND GND VO
+5V_TR
F22 CBWU600
F21 CBWU600
F24 CBWU600OPEN
+5V_TRAN
C240 100uF/10V
C259 0.1uF
L204 CR54/47uH
C244 100uF/16V
C255 0.1uF
+5V_TFT
U21 NCP1117open
IN GND OUT
+3.3V_TFT
C246 10uopen
C247 100u/6.3Vopen
C245 10uopen
C248 220u/6.3Vopen
INV_17V C231 1uF/50V
D24 1N5819
D25 1N5819
C249 10uF/25V
L208 20uH 1210IF200
C233 0.1uF
Q23 3906
R229 1K
D26 RLZ13B
C239 0.1uF
C241 47uF/16V
-10V_TFT
U24 AMS1117-ADJ
+3.3V
C221 47uF/6.3V
C222 0.1uF
VIN ADJ VOUT VOUT
FV18
F201 FB V18
R227 560RF
R219 300RF
C217 0.1uF
C224 100uF/6.3V
C230 47uF/6.3V
6R8uH/CR54
+5V_TRAN L252
INV_17V
D38 1N5819
L209 20uH 1210IF200
Q60 3904
+7.5V_TFT
C256 100uF/6.3V
C257 0.1uF
U26
SHDN FB GND VIN SW
FN5331
C258 47uF/25V
C261 0.1uF
R257 1K
D34 RLZ8.2B
C260 47uF/16V
R255 100K
R256 24K
C263 0.1uF
R254 10K
C264 10uF/25
+17V_TFT
9VIN
+3.3V
PWD_P
PWD_B
V18
CTR_TFT
+5V_TFT
+7.5V_TFT
+17V_TFT
-10V_TFT
GND
+3.3V_TFT

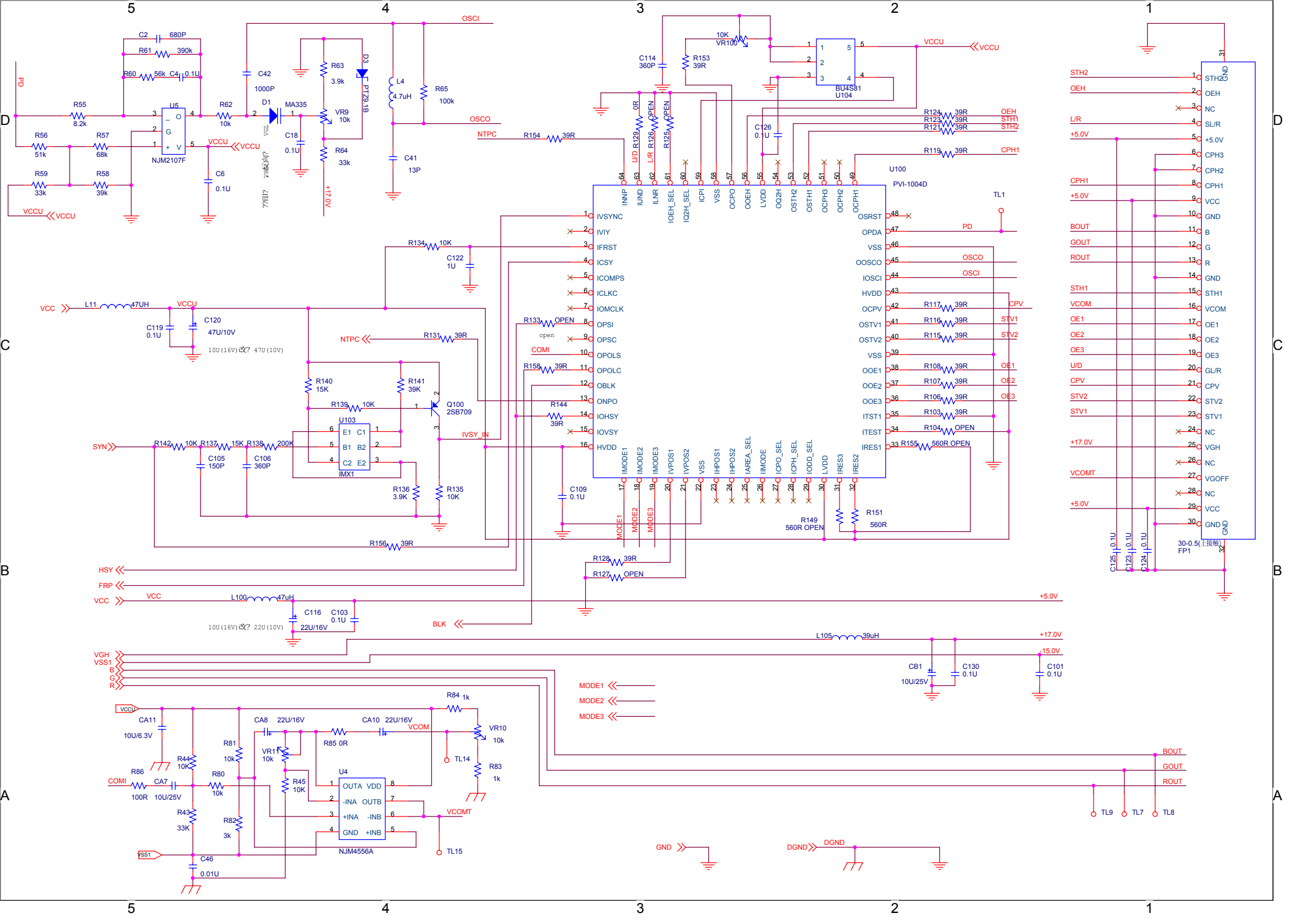

Pin assignment version 1.5


U41
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
DBA0
DBA1
SDCLK
SDCKE
DCS#
DRAS#
DCAS#
DWE#
DQM0
DQM1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
BA0/A13
BA1/A12
CLK
CKE
CS
RAS
CAS
WE
DQML
DQMH
NC
NC
VSS
VSS
VSS
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
VCC
VCC
VCC
VCCQ
VCCQ
VCCQ
VCCQ
VSSQ
VSSQ
VSSQ
VSSQ
SD33
ESMT M12L64164A
A20
R401
R402
0R
R
AA20
A21
R405
R406
AA21
U43
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
WP/ACC
BYTE
VCC
GND1
GND2
CE
OE
WE
RESET
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
FLASH_VCC
R407
10K
R408
10K
PCE#
PRD#
PWR#
C403
0.1uF
(STM29W160)/MX29LV160/MBM29LV160BA(TA)/160TE(BE)-70PFTN(PFCN)
+3.3V
C401
0.1uF
U42
NC
NC
NC
GND
VCC
WP
SCL
SDA
R403
680R
R404
680R
EEPROM 24C02(04)
[3] DQ[0..15]
DQ[0..15]
[3] MA[0..11]
[3] BA[0..1]
[3] DQM[0..1]
[3] DCLK
[3] DCKE
[3] CAS#
[3] RAS#
[3] WE#
[3] CS#
MA[0..11]
BA[0..1]
DQM[0..1]
DCLK
DCKE
CAS#
RAS#
WE#
CS#
[3] PCE#
[3] PRD#
[3] PWR#
[3] A[0..21]
[3] AD[0..7]
PCE#
PRD#
PWR#
A[0..21]
AD[0..7]
[3] SCL
[3] SDA
SCL
SDA
GND
GND
[1,2,3,4,5,6]
+3.3V
+3.3V
GND
GND
F401
FB
+3.3V
SD33
C412
47uF/6.3V
C404
C405
C406
C407
C408
C409
C410
0.1uF
F402
FB
+3.3V
FLASH_VCC
C413
47uF/6.3V
C411
0.1uF
RN41 33R*4
DCS#
DRAS#
DCAS#
DWE#
CS#
RAS#
CAS#
WE#
DBA0
DBA1
SDCKE
SDCLK
R409
R410
R411
R412
33R
BA0
BA1
DCKE
DCLK


RN51 33R*4
ASDAT0
ABCK
ALRCK
ACLK
SDAT0
SBCLK
SLRCK
SACLK
U51
SDATA
DEM/SCLK
LRCK
MCLK
AOUTL
VA
AGND
AOUTR
DAC_ML
VCCDAC
DAC_MR
CS4334
F501=R701
10R 0805
C520 0.01uF
C521 0.1uF
C522 100uF/10V
R700
R556 1K
C544 100uF/10V
R546 1K
C548 0.1uF
C501 10uF/10V
R501 2.4K
R502 6.8K
C503 100pF
R503 12K
C502 390pF
U62A MC33202D
C506 10uF/10V
R505 8.2K
AL_SP
C504 47uF/10V
C505 0.1uF
C509 0.1uF
C510 47uF/6.3V
C511 10uF/10V
R510 2.4K
R511 6.8K
C513 100pF
R512 12K
C512 390pF
U62B MC33202D
C514 10uF/10V
AR_SP
R514 8.2K
C508 10uF/10V
R508 1.8K
R507 100K
A_IN/OUTL
R509 560R
Q51 3904
R518 560R
Q52 3904
C518 10uF/10V
R517 1.8K
R516 100K
A_IN/OUTR
A_MUTE
D51 1N4148
D52 1N4148
R540 22K
C542 220uF/6.3V
R526 470R
Q53 3906
C541 100uF/6.3V
D53 1N4148
R536 560R
R537 4K7
Q54 3906
MUTE_DAC
R539 4K7
Q55 3904
9VIN
+3.3V
+5V
ASPDIF
MUTE_DAC
CTR_TFT
INT/EXT
SVIDEO_Y
SY_TFT
CVBS_TV
GND
ROUT+
SE/BTL
LOUT+
U66
F_TB3GA4.5Z
Q57
9014
R654 4.7K
U85
NJU4052BV
AR_SPEAKER
A_IN/OUTR
AR_SP
C829
C817
C824
C821 10uF/10V AL_SP
C823 10uF/10V AL_SPEAKER
C818 10uF/10V A_IN/OUTL
C822 0.1uF
C819 47uF/10V
R821 4.7K
R823 4.7K
INH B A On Switch
0 0 0 Y0 X0
0 0 1 Y1 X1
0 1 0 Y2 X2
0 1 1 Y3 X3
1 X X None
U53 TPA6011A4PWPR
PGND
ROUT+
ROUT-
SE/BTL
PVDD
HP/LINE
RHPIN
VOLUME
RLINEIN
SEDIFF
RIN
SEMAX
VDD
AGND
LIN
BYPASS
LLINEIN
FADE
LHPIN
SHUTDOWN
LOUT+
LOUT-
PGND
HP/SP
R520 100K
R519 100K
C523 220uF/6.3V
R521 1K
HP_R
HP_L
R522 1K
C533 220uF/6.3V
C529 0.47uF
C524 47uF/10V
C525 0.1uF
C526 0.47uF
C527 0.47uF
C528 0.47uF
C530 47uF/10V
C532 0.1uF
C531 0.47uF
C534 47uF/10V
C535 0.1uF
J8
ST-212C-050-100
J7
ST-212C-050-100
J3
AUDIOL
AUDIOL
AUDIOR
GND
GND
ST-006C-050-300
White
CON15
ROUT+
ROUT-
LOUT+
LOUT-
TH4A(1.25MM)
0123452 67
R544 1K
VOLUME
J4
A-HA1-B103-B20B160B0
SEDIFF
SEMAX
FADE
R523 3K3
R524 1.8K
R525 1.8K
R527 3K3
R529 R
R530 0R
R533 1K
R532 4K7
SHD
MUTE_DAC
R534 4K7
Q58 3904
D54 1N4148
HP/SP
R528 4K7
CTR_TFT
R531 4K7
Q59 3904


Y4
L607 1.8uH
Y/G
C602 22pF
R601 75R
C601 270pF
C603 330pF
Y5
L608 1.8uH
B/Cb/Pb
C605 22pF
R602 75R
C604 270pF
C606 330pF
Y6
L609 1.8uH
R/Cr/Pr
C608 22pF
R603 75R
C607 270pF
C609 330pF
J5
G/Y
G/Y
B/Cb
B/Cb
R/Cr
R/Cr
GND
GND
ST-013
Y1
L601 1.8uH
SVIDEO_Y
C617 22pF
R608 75R
C616 270pF
C618 330pF
Y2
L602 1.8uH
SC_TFT
C620 22pF
R609 75R
C619 270pF
C621 330pF
Y1
Y2
Y3
Y4
Y5
Y6
ASPDIF
9VIN
+5V_TFT
+7.5V_TFT
+17V_TFT
-10V_TFT
HGND
INT/EXT
P/N
SCL
SDA
TIMD1
TIMD2
CVBS_TV
SY_TFT
SVIDEO_Y
GND
+3.3V_TFT
CVBS_TV0
Y3
L605 1.8uH
CVBS_TV
C611 22pF
R604 75R
C610 270pF
C612 330pF
CVBS_TV0
J6
VIDEO
VIDEO
COAX
GND
GND
ST-006C-050-400
Yellow
ASPDIF
C613 0.1uF
R605 75R
R606 75R
C614 100pF
C615 100pF
R607 150R
M1 MARK
M2 MARK
M3 MARK
M4 MARK
M5 MARK
M6 MARK
M7 MARK
M8 MARK
CON8
SDA
SCL
P/N
INT/EXT
TIMD2
TIMD1
F601 CBWU600
SY_TFT
F602 CBGU102
SC_TFT
F603 CBGU102
F604 CBWU600
-10V_TFT
F707 CBWU600
9VIN
L711 22uH PIO54
+3.3V_TFT
F711 OPENCBWU600
F708 CBWU600
+5V_TFT
L703 100uH PIO54
F710 CBWU600
+7.5V_TFT
F712 CBWU600
+17V_TFT
F713 CBWU600
HGND
C710 220uF/6.3V
C711 0.1uF
20 SDA
19 SCL
18 PAL/NTSC
17 INT/EXT
16 TIMD2
15 TIMD1
14 GND
13 SVIDEO_Y
12 SVIDEO_C
11 GND
10 -10V
9 VIN
8 VIN
7 CTR_INV
6 +5V
5 +5V
4 +7.5V
3 +17V
2 HGND
1 HGND
SM20B-SURS-TF(0.8MM)

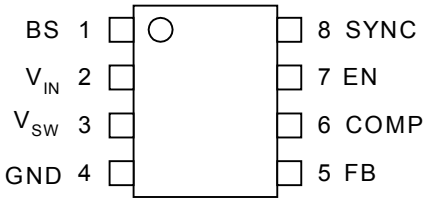

VCC==+5.0V(+/-0.3V)
VDD==+3.3V(+/-0.2V)
VEE==+7.5V(+/-0.2V)
VGH==+17V(+/-1.5V)
VSS==-12V(+/-1.0V)
U1
IR3Y29BM
U3
BU4053FU
This part in control NTSC/PAL exchange
JP1
TH20AW
JP3
TH3AW
Q1
3904
Q2
2SB709
D2
4148


U100
PVI-1004D
NJM2107F
NJM4556A
BU4S81
U104
Q100
2SB709
IMX1
U103
U4
U5
VR100
VR9
VR10
VR11
TL1
FP1
OSCI
OSCO
NTPC
IVSY_IN
BLK
HSY
FRP
SYN
COMI
VCOMT
VCOM
VCC
VCCU
+5.0V
+17.0V
-15.0V
DGND
GND
PD
MODE1
MODE2
MODE3
BOUT
GOUT
ROUT
STH2
OEH
L/R
CPH1
CPH2
CPH3
STH1
VCOM
OE1
OE2
OE3
U/D
CPV
STV2
STV1
VGH
VGOFF
VGL
VSS1
IVSYNC
IVIY
IFRST
ICSY
ICOMPS
ICLKC
IOMCLK
OPSI
OPSC
OPOLS
OPOLC
OBLK
ONPO
IOHSY
IOVSY
HVDD
OSRST
OPDA
VSS
OOSCO
IOSCI
HVDD
OCPV
OSTV1
OSTV2
VSS
OOE1
OOE2
OOE3
ITST1
ITEST
IRES1
INNP
IUND
ILNR
IOEH_SEL
IOE2H_SEL
ICPI
VSS
OCPO
OOEH
LVDD
OQ2H
OSTH2
OSTH1
OCPH3
OCPH2
OCPH1
IMODE1
IMODE2
IMODE3
IVPOS1
IVPOS2
VSS
IHPOS1
IHPOS2
IAREA_SEL
IIMODE
ICPO_SEL
ICPH_SEL
IODD_SEL
LVDD
IRES3
IRES2
R55 8.2k
R56 51k
R57 68k
R58 39k
R59 33k
R60 56k
R61 390k
R62 10k
R63 3.9k
R64 33k
R65 100k
R81 10k
R82 3k
R83 1k
R84 1k
R85 0R
R86 100R
R80 10k
R43 33K
R44 10K
R45 10K
R134 10K
R131 39R
R133 OPEN
R158 39R
R144 39R
R154 39R
R156 39R
R139 10K
R140 15K
R141 39K
R142 10K
R137 15K
R138 200K
R136 3.9K
R135 10K
R153 39R
R129 0R
R126 OPEN
R125 OPEN
R124 39R
R123 39R
R121 39R
R119 39R
R117 39R
R116 39R
R115 39R
R108 39R
R107 39R
R106 39R
R103 39R
R104 OPEN
R155 560R OPEN
R149 560R OPEN
R151 560R
R128 39R
R127 OPEN
C2 680P
C4 0.1U
C6 0.1U
C18 0.1U
C41 13P
C42 1000P
C46 0.01U
C105 150P
C106 360P
C109 0.1U
C114 360P
C116 22U/16V
C103 0.1U
C119 0.1U
C120 47U/10V
C122 1U
C126 0.1U
C130 0.1U
C101 0.1U
CB1 10U/25V
CA11 10U/6.3V
CA7 10U/25V
CA8 22U/16V
CA10 22U/16V
C125 0.1U
C123 0.1U
C124 0.1U
L4 4.7uH
L11 47UH
L100 47uH
L105 39uH
D1 MA335
D3 PTZ9.1B
TL7
TL8
TL9
TL14
TL15

4.Critical Components List

Singing	Appellation
MPS1410	IC
MX29LV800	IC
TPA6011	IC
MT1389DE-B	IC
FN5331	IC
AT5654	IC
MC33202	IC
IR3Y29BM	IC
PVI-1004B/C	IC

5. IC Date Sheet & IC Description



Pin Functions

BS (Pin 1) Bootstrap

This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between V_{SW} and Bootstrap pins to effect a floating supply across the power switch driver. The voltage across C_B is about 5V and is supplied by the internal +5V supply when the V_{SW} pin voltage is low.

V_{IN} (Pin 2) Supply Voltage

The MP1580 operates from a +4.75 to +25V unregulated input. C_{IN} is needed to prevent large voltage spikes from appearing at the input.

V_{SW} (Pin 3) Switch

This connects the inductor to either the V_{IN} through M1 or to GND through M2.

GND (Pin 4) Ground

This pin is the voltage reference for the regulated voltage. For this reason care must be taken in its layout. This node should be placed outside of the D_{SCH} to C_{IN} ground path to prevent switching current spikes to induce voltage noise into the part.

FB (Pin 5) Feedback

An external resistor divider from the output voltage to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillation frequency when the FB voltage is below 650mV.

COMP (Pin 6) Compensation

This node is the output of the transconductance error amplifier and the input to the current comparator. Frequency compensation is done at this node by connecting a series R-C to ground. See the compensation section for exact details.

EN (Pin 7) Enable/UVLO

A voltage greater than 2.495V enables operation. Leave the input unconnected if unused. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from Vin to GND. For complete low current shutdown its needs to be less than 0.7V.

SYNC (Pin 8) Synchronization Input

This pin is used to synchronize the internal oscillator frequency to an external source. There is an internal 11kohm pull down resistor to GND hence leave the input unconnected if unused.

Sync Pin Operation.

The Sync pin driving waveform should be a square wave with a rise time of less than 20ns. Minimum Hi voltage level is 2.7V. Low level is less than 0.8V. The frequency of the external Sync signal needs to be greater than 445 kHz.

A rising edge on the Sync pin forces a reset of the oscillator. The the upper DMOS is switched off immediately if it is not already off. 250nS later the upper DMOS turns on connecting Vsw to Vcc.

Abbr. :

SR : Slew Rate

PU : Pull Up

PD : Pull Down

SMT : Schmitt Trigger

2MA~16MA : Output buffer driving strength.

Pin	Main	Alt.	Type	Description
RF Interface (28)				
226	RFGND18		Ground	Analog ground
227	RFVDD18		Power	Analog power 1.8V
250	NC			
251	NC			
252	OSP		Analog output	RF Offset cancellation capacitor connecting
253	OSN		Analog output	RF Offset cancellation capacitor connecting
254	RFGC		Analog output	RF AGC loop capacitor connecting for DVD-ROM
255	IREF		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS.
256	AVDD3		Power	Analog power 3.3V
1	AGND		Ground	Analog ground
2	DVDA		Analog Input	AC coupled input path A
3	DVDB		Analog Input	AC coupled input path B
4	DVDC		Analog Input	AC coupled input path C
5	DVDD		Analog Input	AC coupled input path D
6	DVDRFIP		Analog Input	AC coupled DVD RF signal input RFIP
7	DVDRFIN		Analog Input	AC coupled DVD RF signal input RFIN
8	MA		Analog Input	DC coupled main-beam RF signal input A
9	MB		Analog Input	DC coupled main-beam RF signal input B
10	MC		Analog Input	DC coupled main-beam RF signal input C
11	MD		Analog Input	DC coupled main-beam RF signal input D
12	SA		Analog Input	DC coupled sub-beam RF signal input A
13	SB		Analog Input	DC coupled sub-beam RF signal input B
14	SC		Analog Input	DC coupled sub-beam RF signal input C
15	SD		Analog Input	DC coupled sub-beam RF signal input D
16	CDFON		Analog Input	CD focusing error negative input
17	CDFOP		Analog Input	CD focusing error positive input
18	TNI		Analog Input	3 beam satellite PD signal negative input
19	TPI		Analog Input	3 beam satellite PD signal positive input

Pin	Main	Alt.	Type	Description
ALPC (4)				
20	MDI1		Analog Input	Laser power monitor input
21	MDI2		Analog Input	Laser power monitor input
22	LDO2		Analog Output	Laser driver output
23	LDO1		Analog Output	Laser driver output
ADC for SACD (5)				
239	ADCVDD3		Power	Analog 3.3V Power for ADC
240	NC			
241	ADCVSS		Ground	Analog ground for ADC
242	NC			
243	NC			
Reference Voltage (3)				
28	V2REFO		Analog output	Reference voltage 2.8V
29	V20		Analog output	Reference voltage 2.0V
30	VREFO		Analog output	Reference voltage 1.4V
Analog Monitor Output (7)				
24	SVDD3		Power	Analog power 3.3V
25	CSO	RFOP	Analog output	1) Central servo 2) Positive main beam summing output
26	RFLVL	RFON	Analog output	1) RFRP low pass, or 2) Negative main beam summing output
27	SGND		Ground	Analog ground
31	FEO		Analog output	Focus error monitor output
32	TEO		Analog output	Tracking error monitor output
33	TEZISLV		Analog output	TE Slicing Level
Analog Servo Interface (6)				
244	RFVDD3		Power	Analog Power
245	RFRPDC		Analog output	RF ripple detect output
246	RFRPAC		Analog Input	RF ripple detect input(through AC-coupling)
247	HRFZC		Analog Input	High frequency RF ripple zero crossing
248	CRTPLP		Analog output	Defect level filter capacitor connecting
249	RFGND		Ground	Analog Power
RF Data PLL Interface (9)				
230	JITFO		Analog output	The output terminal of RF jitter meter.
231	JITFN		Analog Input	The input terminal of RF jitter meter.
232	PLLVSS		Ground	Ground pin for data PLL and related analog circuitry.

Pin	Main	Alt.	Type	Description
233	IDACEXLP		Analog output	Data PLL DAC Low-pass filter
234	PLLVDD3		Power	Power pin for data PLL and related analog circuitry.
235	LPFON		Analog Output	The negative output of loop filter amplifier
236	LPFIP		Analog Input	The positive input terminal of loop filter amplifier.
237	LPFIN		Analog Input	The negative input terminal of loop filter amplifier.
238	LPFOP		Analog Output	The positive output of loop filter amplifier
Motor and Actuator Driver Interface (10)				
34	OP_OUT		Analog output	Op amp output.
35	OP_INN		Analog input	Op amp negative input
36	OP_INP		Analog input	Op amp positive input
37	DMO		Analog Output	Disk motor control output. PWM output.
38	FMO		Analog Output	Feed motor control. PWM output.
39	TROPENPWM		Analog Output	Tray PWM output / Tray open output.
40	PWMOUT1	V_ADIN9	Analog Output	1) 1st General PWM output, or 2) Version AD input 9
41	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator.
42	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
47	FG (Diogital pin)	V_ADIN8	LVTTL 3.3V Input, Schmitt Input, pull up , with analog input path for V_ADIN8	1) Motor Hall sensor input, or 2) Version AD input 8
General Power/Ground (32)				
52,97, 122,152,173, 221	DVDD18		Power	1.8V power pin for internal digital circuitry
43, 85,116,144, 163,216	DVSS		Ground	1.8V Ground pin for internal digital circuitry
46, 73,80,108, 127,141,155, 167,182,212	DVDD3		Power	3.3V power pin for internal digital circuitry
62,94,119, 134,148,161, 223	DVSS		Ground	3.3V Ground pin for internal digital circuitry
204	DVDD3		Power	3.3V power pin Video DAC digital circuitry only
63	APLLCAP		Analog Inout	APLL External Capacitance connection
64	APLLVSS		Ground	Ground pin for audio clock circuitry
65	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
175	NC			

Pin	Main	Alt.	Type	Description
Micro Controller and Flash Interface (48)				
59	HIGHA0		Inout 2~16MA, SR PU	Microcontroller address 8
75	HIGHA1		Inout 2~16MA, SR PU	Microcontroller address 9
74	HIGHA2		Inout 2~16MA, SR PU	Microcontroller address 10
72	HIGHA3		Inout 2~16MA, SR PU	Microcontroller address 11
71	HIGHA4		Inout 2~16MA, SR PU	Microcontroller address 12
70	HIGHA5		Inout 2~16MA, SR PU	Microcontroller address 13
69	HIGHA6		Inout 2~16MA, SR PU	Microcontroller address 14
68	HIGHA7		Inout 2~16MA, SR PU	Microcontroller address 15
91	AD7		Inout 2~16MA, SR	Microcontroller address/data 7
88	AD6		Inout 2~16MA, SR	Microcontroller address/data 6
87	AD5		Inout 2~16MA, SR	Microcontroller address/data 5
86	AD4		Inout 2~16MA, SR	Microcontroller address/data 4
84	AD3		Inout 2~16MA, SR	Microcontroller address/data 3
83	AD2		Inout 2~16MA, SR	Microcontroller address/data 2
82	AD1		Inout 2~16MA, SR	Microcontroller address/data 1
81	AD0		Inout 2~16MA, SR	Microcontroller address/data 0
93	IOA0		Inout 2~16MA, SR PU	Microcontroller address 0 / IO

Pin	Main	Alt.	Type	Description
78	IOA1		Inout 2~16MA, SR PU	Microcontroller address 1 / IO
53	IOA2		Inout 2~16MA, SR PU	Microcontroller address 2 / IO
54	IOA3		Inout 2~16MA, SR PU	Microcontroller address 3 / IO
55	IOA4		Inout 2~16MA, SR PU	Microcontroller address 4 / IO
56	IOA5		Inout 2~16MA, SR PU	Microcontroller address 5 / IO
57	IOA6		Inout 2~16MA, SR PU	Microcontroller address 6 / IO
58	IOA7		Inout 2~16MA, SR PU	Microcontroller address 7 / IO
67	A16		Output 2~16MA, SR	Flash address 16
92	A17		Output 2~16MA, SR	Flash address 17
60	IOA18		Inout 2~16MA, SR SMT	Flash address 18 / IO
61	IOA19		Inout 2~16MA, SR SMT	Flash address 19 / IO
76	IOA20		Inout 2~16MA, SR SMT	Flash address 20 / IO
89	IOA21	V_ADIN0	Inout 2~16MA, SR SMT	1) Flash address 21 / IO 2) While External FLASH size <= 2MB: I) Version AD input port 0, or II) GPIO
90	ALE		Inout 2~16MA, SR PU, SMT	Microcontroller address latch enable
79	IOOE#		Inout 2~16MA, SR SMT	Flash output enable, active low / IO
66	IOWR#		Inout 2~16MA, SR SMT	Flash write enable, active low / IO

Pin	Main	Alt.	Type	Description
77	IOCS#		Inout 2~16MA, SR PU, SMT	Flash chip select, active low / IO
95	UWR#		Inout 2~16MA, SR PU, SMT	Microcontroller write strobe, active low
96	URD#		Inout 2~16MA, SR PU, SMT	Microcontroller read strobe, active low
98	UP1_2		Inout 4MA, SR PU, SMT	Microcontroller port 1-2
99	UP1_3		Inout 4MA, SR PU, SMT	Microcontroller port 1-3
100	UP1_4		Inout 4MA, SR PU, SMT	Microcontroller port 1-4
101	UP1_5		Inout 4MA, SR PU, SMT	Microcontroller port 1-5
102	UP1_6	SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-6 2) I^2C clock pin
103	UP1_7	SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-7 2) I^2C data pin
104	UP3_0	RXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-0 2) 8032 RS232 RXD
105	UP3_1	TXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-1 2) 8032 RS232 TXD
106	UP3_4	RXD SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-4 2) Hardwired RD232 RXD 3) I^2C clock pin
107	UP3_5	TXD SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-5 2) Hardwired RD232 TXD 3) I^2C data pin
111	IR		Input SMT	IR control signal input
112	INT0#		Inout 2~16MA, SR PU, SMT	Microcontroller external interrupt 0, active low
Audio interface (14)				

Pin	Main	Alt.	Type	Description
208	SPMCLK	SCLK0	Inout	1) Audio DAC master clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 clock pin II) GPIO
209	SPDATA	SDIN0	Inout	1) Audio data of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 data-in II) GPIO
210	SPLRCK	SDO0	Inout	1) Audio left/right channel clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 data-out II) GPIO
211	SPBCK	SDCS0 ASDATA5	Inout	1) Audio bit clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 chip select II) Audio serial data 5 part I : DSD data sub-woofer channel or Microphone output III) GPIO
213	ALRCK		Inout 4MA, PD, SMT	1) Audio left/right channel clock 2) Trap value in power-on reset: I) 1 : use external 373 II) 0: use internal 373
214	ABCK	Fs64	Output 4MA	1) Audio bit clock 2) Phase de-modulation
215	ACLK		Inout 4MA	Audio DAC master clock
217	ASDATA0		Inout 4MA PD SMT	1) Audio serial data 0 (Front-Left/Front-Right) 2) DSD data left channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation
218	ASDATA1		Inout 4MA PD SMT	1) Audio serial data 1 (Left-Surround/Right-Surround) 2) DSD data right channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) GPIO
219	ASDATA2		Inout 4MA PD SMT	1) Audio serial data 2 (Center/LFE) 2) DSD data left surround channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) GPIO

Pin	Main	Alt.	Type	Description
220	ASDATA3		Inout 4MA PD SMT	1) Audio serial data 3 (Center-back/ Center-left-back/Center-right-back, in 6.1 or 7.1 mode) 2) DSD data right surround channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) GPIO
222	ASDATA4	INT1#	Inout 4MA PD SMT	1) Audio serial data 4 (Down-mixed Left/Right) 2) DSD data center channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) Microcontroller external interrupt 1 II) GPIO
224	MC_DATA	INT2#	Inout	1) Microphone serial input 2) While not support Microphone: I) Microcontroller external interrupt 2 II) GPIO
225	SPDIF		Output 2~16MA, SR : ON/OFF	SPDIF output
Video Interface (18)				
189	DACVDDC		Power	3.3V power pin for VIDEO DAC circuitry
190	VREF		Analog	Bandgap reference voltage
191	FS		Analog	Full scale adjustment
192	YUV0	CIN	Output 4MA, SR	1) Video data output bit 0 2) Compensation capacitor
193	DACVSSC		Ground	Ground pin for VIDEO DAC circuitry
194	YUV1	Y	Output 4MA, SR	1) Video data output bit 1 2) Analog Y output
195	DACVDDB		Power	3.3V power pin for VIDEO DAC circuitry
196	YUV2	C	Output 4MA, SR	1) Video data output bit 2 2) Analog chroma output
197	DACVSSB		Ground	Ground pin for VIDEO DAC circuitry
198	YUV3	CVBS	Output 4MA, SR	1) Video data output bit 3 2) Analog composite output
199	DACVDDA		Power	3.3V power pin for VIDEO DAC circuitry
200	YUV4	Y/G	Output 4MA, SR	1) Video data output bit 4 2) Green or Y
201	DACVSSA		Ground	Ground pin for VIDEO DAC circuitry
202	YUV5	B/Cb/Pb	Output 4MA, SR	1) Video data output bit 5 2) Blue or CB

Pin	Main	Alt.	Type	Description
203	YUV6	R/Cr/Pr	Output 4MA, SR	1) Video data output bit 6 2) Red or CR
205	VSYN	V_ADIN1	Inout 4MA, SR SMT	1) Vertical sync input/output 2) While no External TV-encoder: I) Vertical sync for video-input II) Version AD input port 1 III) GPIO
206	YUV7	INT3# ASDATA5	Inout 4MA, SR SMT	1) Video data output bit 7 2) While no External TV-encoder: I) Microcontroller external interrupt 3 II) Audio serial data 5 part II : DSD data sub-woofer channel or Microphone output III) GPIO
207	HSYN	INT4# V_ADIN2	Inout 4MA, SR SMT	1) Horizontal sync input/output 2) While no External TV-encoder: I) Horizontal sync for video-input II) Microcontroller external interrupt 4 III) Version AD input port 2 IV) GPIO
MISC (8)				
44	NC			
45	NC			
110	PRST#		Input PU, SMT	Power on reset input, active low
109	ICE		Input PD, SMT	Microcontroller ICE mode enable
228	XTALO		Output	27M crystal out
229	XTALI		Input	27M crystal in
Dram Interface (63) (Sorted by position)				
188	NC			
187	NC			
186	NC			
185	NC			
184	NC			
183	NC			
181	NC			
180	NC			
179	DQM2		Inout Pull-Up	GPIO
178	DQM3		Inout Pull-Up	GPIO
177	RD24		Inout Non-pull	GPIO

Pin	Main	Alt.	Type	Description
176	RD25		Inout Non-pull	GPIO
174	RD26		Inout Non-pull	GPIO
172	NC			
171	NC			
170	RD29		Inout Non-pull	GPIO
169	RD30		Inout Pull-Up	GPIO
168	RD31		Inout Pull-Up	GPIO
166	RA4		Inout	DRAM address 4
165	RA5		Inout	DRAM address 5
164	RA6		Inout	DRAM address 6
162	RA7		Inout	DRAM address 7
160	RA8		Inout	DRAM address 8
159	RA9		Inout	DRAM address 9
158	RA11	GPIO	Inout Pull-Down	3) DRAM address bit 11 4) While using DRAM size <=4MB: I) GPIO
157	CKE		output	DRAM clock enable
156	RCLK		Inout	Dram clock
154	NC			
153	NC			
151	RA3		Inout	DRAM address 3
150	RA2		Inout	DRAM address 2
149	RA1		Inout	DRAM address 1
147	RA0		Inout	DRAM address 0
146	RA10		Inout	DRAM address 10
145	BA1		Inout	DRAM bank address 1
143	BA0		Inout	DRAM bank address 0
142	RCS#		output	DRAM chip select, active low
140	RAS#		output	DRAM row address strobe, active low
139	CAS#		output	DRAM column address strobe, active low
138	RWE#		output	DRAM Write enable, active low
137	DQM1		Inout	Data mask 1
136	DQS1		Inout Non-pull	GPIO
135	RD8		Inout	DRAM data 8
133	RD9		Inout	DRAM data 9
132	RD10		Inout	DRAM data 10
131	RD11		Inout	DRAM data 11
130	RD12		Inout	DRAM data 12
129	RD13		Inout	DRAM data 13
128	RD14		Inout	DRAM data 14

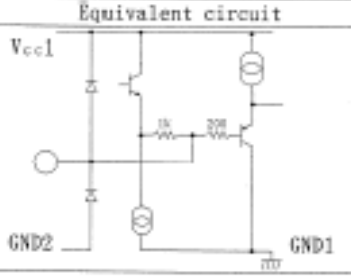
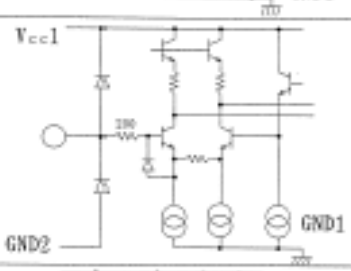
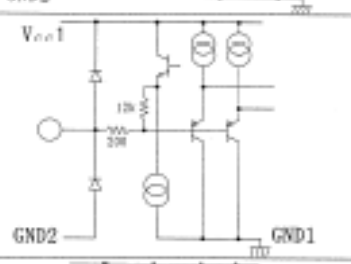
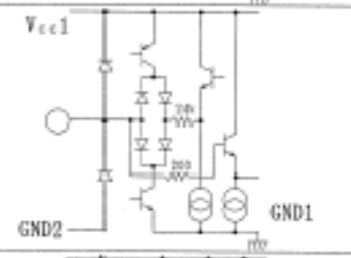
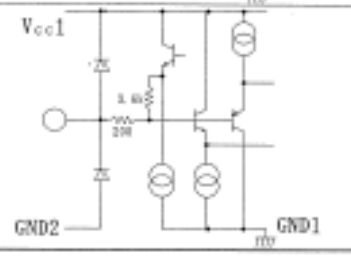
Pin	Main	Alt.	Type	Description
126	RD15		Inout	DRAM data 15
125	RD0		Inout	DRAM data 0
124	RD1		Inout	DRAM data 1
123	RD2		Inout	DRAM data 2
121	RD3		Inout	DRAM data 3
120	RD4		Inout	DRAM data 4
118	RD5		Inout	DRAM data 5
117	RD6		Inout	DRAM data 6
115	RD7		Inout	DRAM data 7
114	DQS0		Inout Non-pull	GPIO
113	DQM0		Inout	Data mask 0
JTAG Interface(4)				
48	TDI	V_ADIN4	Inout	1) Serial interface port 3 data-out 2) Version AD input port 4 3) GPIO
49	TMS	V_ADIN5	Inout	1) Serial interface port 3 data-in 2) Version AD input port 5 3) GPIO
50	TCK	V_ADIN6	Inout	1) Serial interface port 3 clock pin 2) Version AD input port 6 3) GPIO
51	TDO	V_ADIN7	Inout	1) Serial interface port 3 chip-select 2) Version AD input port 7 3) GPIO

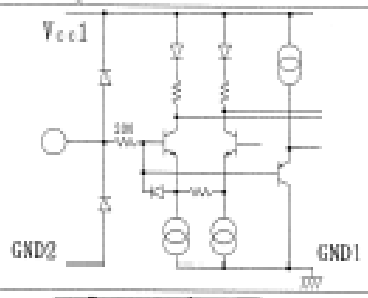
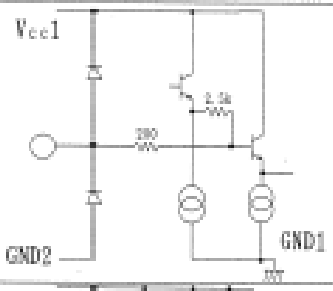
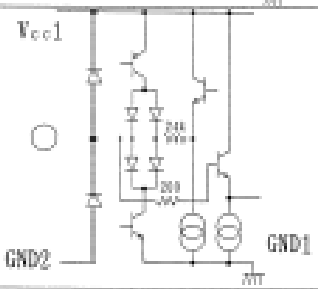
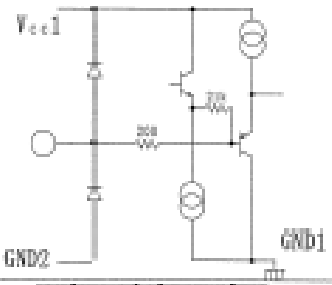
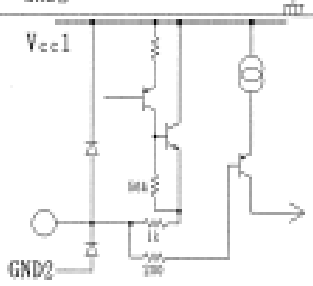
Note:

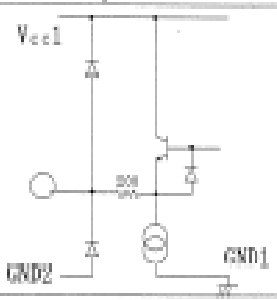
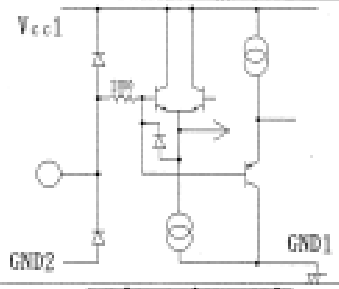
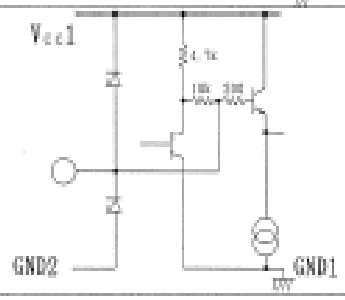
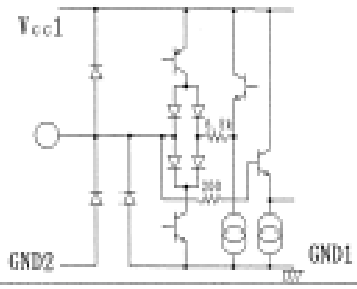
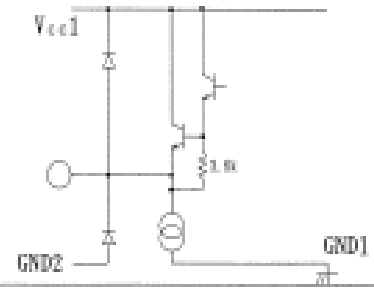
1. The Main column is the main function, Alt. Means alternative function.
2. The multi-function GPIO pins are set to green characters.
3. The video input port and external TV encoder mode can not both use CCIR-601 mode, at least one of them should be in CCIR-656 mode.
4. Following is a summary of modified pins.
   (a) Pin 44, 45, 153, 154, 171, 172, 175, 180, 181, 183, 184, 185, 186, 187, 188, 240, 242, 243, 250, 251 are NC pins.
   (b) Pin 114, 136, 168, 169, 170, 174, 176, 177, 178, 179 will be used as GPIO only.
   (c) Pin 48, 49, 50, 51 are no longer for JTAG functions.
   (d) V_ADIN3 (pin 153) is not available.
   (e) Pin 43 used as 1.8V ground pin for internal digital circuitry. Pin 46 used as 3.3V power pin for internal digital circuity.

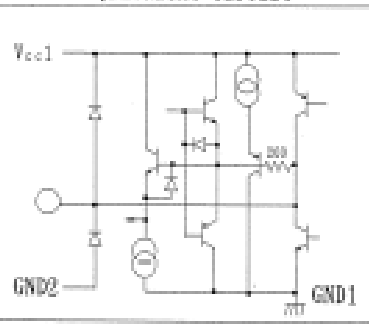
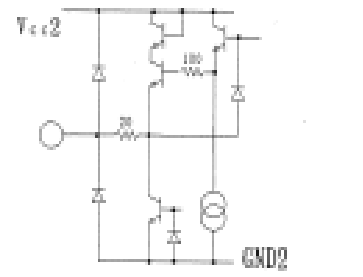
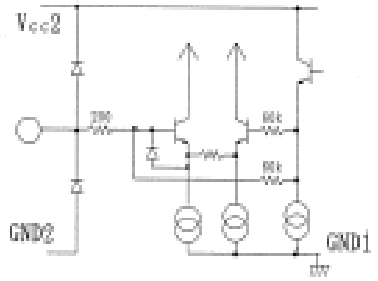
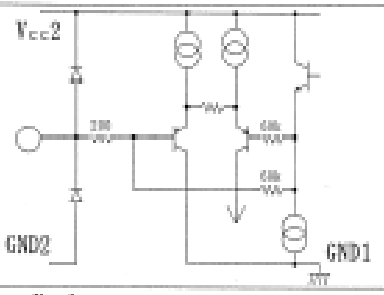
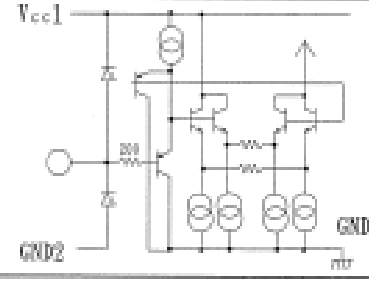
IR3Y29BM Pin Description

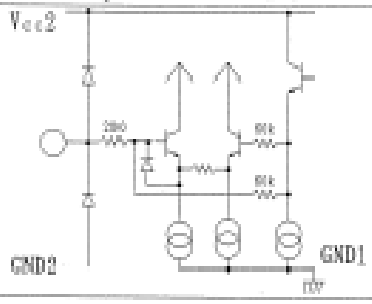
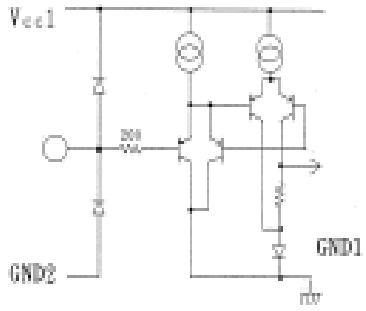
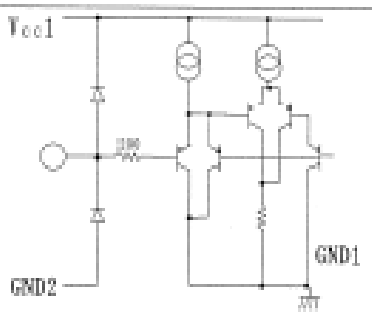
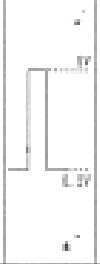
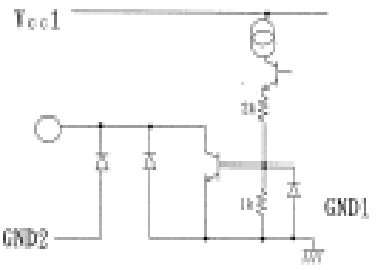
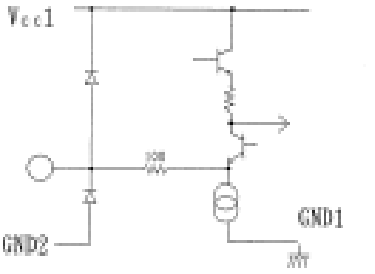
5. Description of Terminals (Vcc1=5.0V/Vcc2=7.5V These voltage are typical value.)

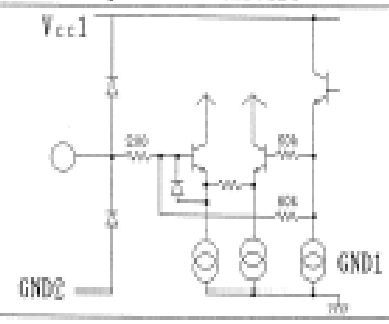
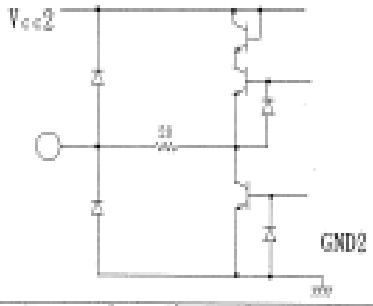
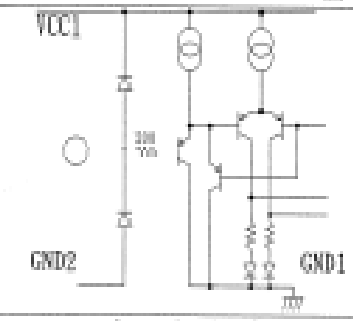
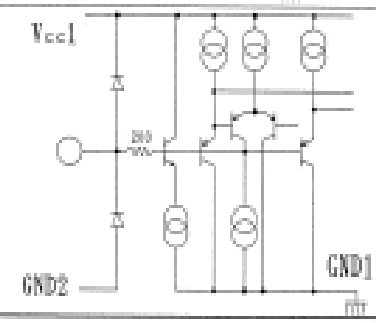
Pin. No.	Term. Name	Voltage	Equivalent circuit	Description
1	TRAP	2.2V		This terminal is connected to the TRAP filter. Output impedance:1kΩ
2	CONTRAST	1.1V ~3.7V		The DC voltage applied to this terminal adjusts the contrast of the composite or Y/C video signal.
3	VIDEO IN	2.2V		Input the composite video signal to this terminal. (In case of using the Y/C video signal, input the luminance signal.)
4	IDENT FILTER	1.0V -		This terminal is connected to the IDENT detection filter.
5	C IN	2.7V		In case of using the Y/C video signal, input the chrominance signal. In case of using the composite video signal, connect this terminal to the ground.

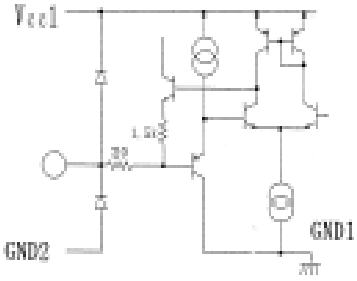
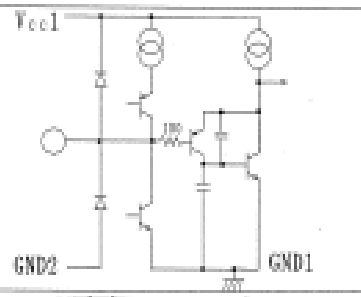
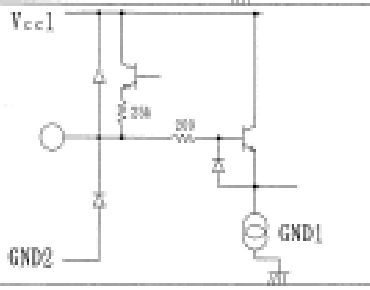
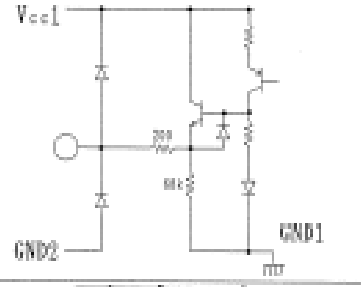
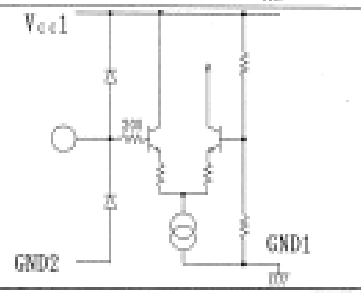
Term. No.	Term. Name	Voltage	Equivalent Circuit	Description
6	COLOR	1.8V ~4.1V		The DC voltage applied to this terminal adjusts the color gain.
7	BURST OUT	3.5V		In case of the PAL mode, this terminal is connected to the burst cleaning coil.
8	KILLER FILTER	1.7V		This terminal is connected to the KILLER detection filter.
9 10	R-Y B-Y	2.2V		Input the chrominance signal for the PAL demodulate circuit.
11	ACC FILTER	1.8V		This terminal is connected to the ACC detection filter.

Term. No.	Term. Name	voltage	Equivalent Circuit	Description
12	CHROMA OUT	2.7V		This terminal outputs the chrominance signal whose color gain has been adjusted and whose burst signal has been removed.
13	TINT	0V ~5V		The voltage applied to this terminal adjusts the tint. This terminal also switches between the NTSC mode and the PAL mode. In case of the PAL mode, connect this terminal to the ground.
14	VCO IN	4.2V		The input terminal of the VCO circuit.
15	APC FILTER	2.6V		This terminal is connected to the APC detection filter.
16	VCO OUT	2.2V		The output terminal of the VCO circuit.
17, 18	GND1, 2	0V		The terminals of GND1 and GND2 are not connected together. Be sure that these terminals should be connected with the same voltage.

Term. No.	Term. Name	Voltage	Equivalent Circuit	Description
20 22 25	R DC DET G DC DET B DC DET	2.3V		This terminal is connected to the capacitor that smooths and holds the DC voltage of the RGB outputs. Because of the high impedance, use low leakage current capacitor.
19 21 24	R OUT G OUT B OUT	$\frac{Vcc1}{2}$ ≈2.5V		Output terminal of the RGB signals.
23	Vcc2			Connect to the power supply for the RGB outputs.
26	GAMMA 2	1.2V ~3.5V		The DC voltage applied to this terminal adjusts the γ2 point. This terminal is pre-set inside the IC.
28	RGB AMPLITUDE ADJUST	1.2V ~3.5V		The DC voltage applied to this terminal adjusts the amplitude (BLK-BLK) of the RGB output signals and the dynamic range. This terminal is preset inside the IC.
27	GAMMA 0	1.2V ~3.5V		The DC voltage applied to this terminal adjusts γ0 point. This terminal is preset inside the IC.
29	BRIGHT	0.7V ~2.6V		The DC voltage applied to this terminal adjusts the position of the gamma correction curve and the amplitude of the common voltage.

Term. No.	Term. Name	voltage	Equivalent Circuit	Description
30 31	SUB BRIGHT B SUB BRIGHT R	1.0V ~3.5V		The DC voltage applied to these terminals adjust the brightness of the R and B signals finely by moving the gamma correction curve. These terminals are preset inside the IC.
32	COMMON FRP			Input the switching signal of the common output.
33	FRP			Input the inverting signal of the RGB outputs. "LOW":Inverting. "HI" :Not inverting.
34	SYNC IN			Input the horizontal synchronizing pulse.(Active Low) In case of the PAL mode, inner flip-flop switches at the rising edge of the input pulse.
35	SYNC OUT			Outputs the composite synchronizing pulse separated by the SYNC-separation circuit. (Active High) The output is provided by an open collector circuit.
36	SYNC SEP	2.0V		The input terminal of the video signal for the SYNC-separation circuit.

Term.No.	Term. Name	Voltage	Equivalent Circuit	Description
37	COMMON AMPLITUDE ADJUST	1.0V ~3.5V		The DC voltage applied to this terminal adjusts the amplitude of the COM output. This terminal is preset inside the IC.
38	COMMON OUT			The output terminal of the COM signal.
39	SW			Input the video source selection signal. Give the "Low" level in case of the composite or Y/C input, and give the "High" level or open in case of the RGB inputs.
40 41 42	B IN G IN R IN	2.2V		The input terminal of the RGB signals. The signal is required to be AC coupled.

Term.No.	Term. Name	Volage	Equivalent Circuit	Description
43	$V_{cc}1$			Connect to the power supply.
44	F ADJ	1.3V		The resistor between this terminal and the ground adjusts the frequency characteristic of the inner filters. The resistor of 18k ohms is recommended for the both mode. Resistance accuracy:±2% Temp. Stability:±200ppm/℃
45	CLAMP	2.4V		Connect the capacitor that clamps the pedestal level of the luminance signal. Because of the high impedance, use the low leackage carrent capacitor.
46	AGC FILTER	2.9V		Connect the AGC detection filter for luminance signal.
47	AGC OUT	0.75V ~3.1V		This terminal outputs the AGC detection voltage of the luminance signal. The output voltage increases with the increase of the AGC gain.
48	PICTURE	1.6V ~3.6V		The DC voltage applied to this terminal adjusts the frequency characteristic of the luminance signal. The outline is emphasized by reducing the voltage of this terminal.

3. Pin assignment

pin No.	pin name	I/O	Remarks	pin No.	pin name	I/O	Remarks
1	ivsync	I	schimtt	33	ires1	I	pull_down
2	iviy	I	schimtt	34	itest	I	pull_up
3	ifrst	I	schimtt	35	itst1	I	AC/DC test
4	icsy	I	schimtt	36	ooe3	O	1mA
5	icomps	I	pull_up	37	ooe2	O	1mA
6	iclkc	I	pull_up	38	ooe1	O	1mA
7	iomclk	I/O	Bi dir.(3mA)	39	VSS		
8	opsi	O	1mA	40	ostv2	O	3_state(1mA)
9	opsc	O	1mA	41	ostv1	O	3_state(1mA)
10	opols	O	3mA	42	ocpv	O	3mA
11	opolc	O	3mA	43	HVDD		5.0V
12	oblk	O	1mA	44	iosci	I	xin (25Mhz)
13	onpo	O	1mA	45	oosco	O	xout(25Mhz)
14	iohsy	I/O	Bi dir.(3mA)	46	VSS		
15	iovsy	I/O	Bi dir(3mA).	47	opda	O	3_state(3mA)
16	HVDD		5.0V	48	osrst	O	1mA
17	imode1	I	pull_down	49	ocph1	O	3mA
18	imode2	I	pull_down	50	ocph2	O	3mA
19	imode3	I	pull_down	51	ocph3	O	3mA
20	ivpos1	I	pull_up	52	osth1	O	3_state(1mA)
21	ivpos2	I	pull_up	53	osth2	O	3_state(1mA)
22	VSS			54	oq2h	O	3mA
23	ihpos1	I	pull_up	55	LVDD		3.3V
24	ihpos2	I	pull_up	56	ooeh	O	3mA
25	iarea_sel	I	pull_up	57	ocpo	O	3mA
26	iimode	I	pull_up	58	VSS		
27	icpo_sel	I	pull_up	59	icpi	I	schmitter
28	icph_sel	I	pull_up	60	iq2h_sel	I	pull_up
29	iodd_sel	I	pull_up	61	ioeh_sel	I	pull_up
30	LVDD		3.3V	62	ilnr	I	pull_up
31	ires3	I	pull_down	63	iund	I	pull_up
32	ires2	I	pull_down	64	innp	I	pull_up

4. Pin Description

No.	Symbol	I/O	Description	Remark
1	ivsync	I	vertical sync signal in composite sync mode (low active)	
2	iviy	I	vertical sync signal in separate sync mode(low active)	
3	ifrst	I	reset pin in ASIC 1) ifrst = "H" : Normal state 2) ifrst = "L" : Reset state	
4	icsy	I	select composite signal/horizontal signal 1) icomps = "H" : icsy is composite sync signal (high active) 2) icomps = "L" : icsy is horizontal sync signal(low active)	
5	icomps	I	select composite sync mode/separate sync mode 1) icomps = "H" : composite sync mode 2) icomps = "L" : separate sync mode	Note1)
6	iclkc	I	select PLL mode/external clock mode 1) iclkc = "H" : PLL mode 2) iclkc = "L" : external clock mode	Note1)
7	iomclk	I/O	input clock signal (external clock mode) 1) iclkc = "H" : This signal will be ground 2) iclkc = "L" : This signal will be external input ternimal	
8	opsi	O	control decorder chip pin	Fig.9
9	opsc	O	control Dimming for inverter	Fig.10
10	opols	O	polarity alternating signal for video	
11	opolc	O	polarity alternating signal for Vcom	
12	oblk	O	blanking control pin 1) oblk ="H" : blanking display (black) 2) oblk ="L" : normal display	Fig.8
13	onpo	O	auto detect pin for NTSC/PAL 1) onpo ="H" : NTSC 2) onpo ='L" : PAL	Note2)
14	iohsy	I/O	input/output horizontal sync. signal (low active) 1) iclkc = "H" : This signal outputs horizontal sync. signal 2) iclkc = "L" : This signal will be external horizontal sync. Input.	
15	iovsy	I/O	input/output vertical sync. signal (low active) 1) iclkc = "H" : This signal outputs vertical sync. signal 2) iclkc = "L" : This signal will be external vertical sync. Input.	
16	HVDD	-	high voltage power (5.0 V or 3.3V)	Note3)
17 18 19	imode1 imode2 imode3	I I I	select display mode (1440, 1200 mode only)	Note4)

imode1	imode2	imode3	Description
L	L	L	Full mode
H	L	L	Normal center mode
L	H	L	Normal wide mode
H	H	L	Zoom1 mode
L	L	H	Zoom2 mode
H	L	H	Normal left mode
L	H	H	Normal right mode
H	H	H	Zoom3 mode

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Remark</th></tr>
<tr><td>20
21</td><td>ivpos1
ivpos2</td><td>I
I</td><td>select vertical start line
<table>
<tr><th>ivpos2</th><th>ivpos1</th><th>NTSC</th><th>PAL</th></tr>
<tr><td>L</td><td>L</td><td>20</td><td>26</td></tr>
<tr><td>L</td><td>H</td><td>21</td><td>28</td></tr>
<tr><td>H</td><td>L</td><td>22</td><td>30</td></tr>
<tr><td>H</td><td>H</td><td>23</td><td>31</td></tr>
</table></td><td></td></tr>
<tr><td>22</td><td>VSS</td><td>-</td><td>Ground</td><td></td></tr>
<tr><td>23
24</td><td>ihpos1
ihpos2</td><td>I
I</td><td>select horizontal start point (iclkc ="L" only, ext clock mode)
<table>
<tr><th>ihpos2</th><th>ihpos1</th><th>1440</th><th>1200</th><th>960</th></tr>
<tr><td>L</td><td>L</td><td>100</td><td>85</td><td>67</td></tr>
<tr><td>L</td><td>H</td><td>101</td><td>86</td><td>68</td></tr>
<tr><td>H</td><td>L</td><td>102</td><td>87</td><td>69</td></tr>
<tr><td>H</td><td>H</td><td>103</td><td>88</td><td>70</td></tr>
</table></td><td>Note5)</td></tr>
<tr><td>25</td><td>iarea_sel</td><td>I</td><td>select display range
1) iarea_sel = "H" : The display range is 50.01us (NTSC)
2) iarea_sel = "L" : The display range is 48.00us (NTSC)</td><td>Note1)</td></tr>
<tr><td>26</td><td>iimode</td><td>I</td><td>select simultaneous mode/sequential mode
1) iimode ="H" : simultaneous mode (stripe arrangement)
2) iimode ="L" : sequential mode (delta arrangement)</td><td>Note1)</td></tr>
<tr><td>27</td><td>icpo_sel</td><td>I</td><td>select horizontal position adjust (iclkc = "H" only)
1) icpo_sel = "H" : hor. Position adjustment is normal
2) icpo_sel = "L" : hor.position adjustment is more wide</td><td>Note1)</td></tr>
<tr><td>28</td><td>icph_sel</td><td>I</td><td>select ocph1,2,3 phase (delta arrangement module only)
1) icph_sel = "H" : PVI's arrangement
2) icph_sel = "L" : another company's arrangement</td><td>Note1)
Note6)</td></tr>
<tr><td>29</td><td>iodd_sel</td><td>I</td><td>select falling edge of iovsy's position (NTSC, composite sync onl
1) iodd_sel = "H" : iovsy's phase difference is 1.5H (even field)
2) iodd_sel = "L" : iovsy's phase difference is 0.5H (even field)</td><td>Note1)</td></tr>
<tr><td>30</td><td>LVDD</td><td>-</td><td>low voltage power (3.3V only)</td><td></td></tr>
<tr><td>31
32
33</td><td>ires3
ires2
ires1</td><td>I
I
I</td><td>select resolution mode
<table>
<tr><th>ires1</th><th>ires2</th><th>ires3</th><th>resolution mode</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>1200 * 234</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>-</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>-</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>240 * 234</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>480 * 234</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>960 * 234</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>720 * 234</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>1440 * 234</td></tr>
</table></td><td></td></tr>
<tr><td>34</td><td>itest</td><td>I</td><td>select test mode
1) itest = "H" : normal mode
2) itest = "L" : test mode</td><td>Note1)</td></tr>
</table>

No.	Symbol	I/O	Description	Remark
35	itst1	I	select AC/DC test 1) itst1 = "H" : AC/DC test mode 2) itst1 = "L" : normal mode	
36 37 38	ooe3 ooe2 ooe1	O O O	output enable control signal for gate driver ooe1,2,3 ="H" : gate output => Vee 1) ooe1 controls 1 4 7 10 --- 238 lines 2) ooe2 controls 2 5 8 11 --- 239 lines 3) ooe3 controls 3 6 9 12 --- 240 lines	note7)
39	VSS	-	Ground	
40	ostv2	O	gate driver start pulse 1) iund = "H" : ostv2 is in high impedance state 2) iund = "L" : ostv2 is output pin of start pulse	note7)
41	ostv1	O	gate driver start pulse 1) iund = "H" : ostv1 is output pin of start pulse 2) iund = "L" : ostv1 is in high impedance state	note7)
42	ocpv	O	gate driver shift clock	
43	HVDD	-	high voltage power (5.0 V or 3.3V)	Note3)
44	iosci	I	input for clock oscillator circuit	
45	oosco	O	output for clock oscillator circuit	
46	VSS	-	Ground	
47	opda	O	output for phase comparative signal for PLL circuit	
48	osrst	O	reset source driver IC (active high)	
49	ocph1	O	source driver shift clock #1	
50	ocph2	O	source driver shift clock #2 1) iimode = "H" : ochp2 is always high signal (stripe arrangement) 2) iimode = "L" : ocph2 is shift clock (delta arrangement)	
51	ocph3	O	source driver shift clock #3 1) iimode = "H" : ochp3 is always low signal (stripe arrangement) 2) iimode = "L" : ocph3 is shift clock (delta arrangement)	
52	osth1	O	source driver start pulse 1) ilnr = "H" : osth1 is output pin of start pulse 2) ilnr = "L" : osth1 is in high impedance state	Note8)
53	osth2	O	source driver start pulse 1) ilnr = "H" : osth2 is in high impedance state 2) ilnr = "L" : osth2 is output pin of start pulse	Note8)
54	oq2h	O	pin of RGB output data order on no rotation mode 1) iimode ="H" : no use (low) 2) iimode ="L" : use (delta arrangement)	
55	LVDD	-	low voltage power (3.3V only)	
56	ooeh	O	output enable control signal for source driver 1) ioeh_sel = "H" : ooeh is active low 2) ioeh_sel = "L" : ooeh is active high	
57	ocpo	O	output for horizontal position adjustment	
58	VSS	-	Ground	
59	icpi	I	input for horizontal position adjustment	

No.	Symbol	I/O	Description	Remark
60	iq2h_sel	I	select oq2h phase (delta arrangement only) 1) iq2h_sel = "H" : PVI's arrangement 2) iq2h_sel = "L" : another company's arrangement	Note1) note6)
61	ioeh_sel	I	select perioty of ooeh 1) ioeh_sel = "H" : ooeh is active low 2) ioeh_sel = "L" : ooeh is active high	Note1)
62	ilnr	I	select left/right direction 1) ilnr = "H" : normal scan 2) ilnr = "L" : reverse scan	Note1) Note8)
63	iund	I	select up/down direction 1) iund = "H" : normal scan 2) iund = "L" : reverse scan	Note1) Note7)
64	innp	I	select NTSC/PAL 1) ilnr = "H" : normal scan 2) ilnr = "L" : reverse scan	Note1)

Note1) Those pins are Normally pull-up
Note2) If use auto detection, this pin must connect innp
Note3) If you want to use 5V's I/O signal, It must connect 5V's Voltage,
otherwise, if you want to use 3.3V's I/O signal, it must connect 3.3V's voltage
Note4) Those pins are Normally pull-down
Note5) This count means No.of input clock from the falling edge of iohsy
Note6) If you use another company's TFT LCD module, please contact PVI.
Note7) iund controls up/down direction
1) iund = "H" : ostv1 → G1(ooe1) → G2(ooe2) → G3(ooe3) → G4(ooe1) → G5(ooe1) → --- → G238(ooe1) → G239(ooe2) → G240(ooe3) → ostv2
2) iund = "L" : ostv1 ← G1(ooe1) ← G2(ooe2) ← G3(ooe3) ← G4(ooe1) ← G5(ooe1) ← --- ← G238(ooe1) ← G239(ooe2) ← G240(ooe3) ← ostv2
Note8) ilnr controls left/right direction
1) ilnr = "H" : osth1 → ----- → osth2
2) ilnr = "L" : osth1 ← ------ ← osth2

6.Service Tools and Equipment

6.1Service Tools and Equipment Table

Application	Name
General	DVD Testing Disc
	General Tools（screwdriver etc.）
Confirm	CD Testing Disc
	VCD Testing Disc
Adjust	Oscillograph
	Probes
	AV Cables
	TV Monitor
Grounding for electrostatic breakdown	Searing-iron
	Antistatic wrist strap
	Conductive material（steel sheet）

6.2 Storing and Handling Test Discs

It is important for a DVD testing disc keeping its surface precise. Please care for storing and using it.

1. Do not place the disc on worktable directly after using.
2. Do not store discs in places subject to direct sunlight or near heat sources.

3. Do not place the disc on a glass surface. It may damage the disc. If this happened, please use a new testing disc adjust DVD player precision.

6.3 Notes

PLEASE READ ALL NOTES GIVEN IN THIS MANUAL.

■ **Locate**

- Place the unit on a firm, flat surface.
- Do not place in a high temperature (upwards of 35℃) or high wet (upwards of 90 percent) area.
- Do not place in an area with a lot of dust.
- Keep away from direct sunlight &domestic heating equipment.

■ **Do not fall any objects into the unit.**

- Care should be taken so that liquids are not spilled into the unit openings. Such situations could result in fire or electrical shock.
- Keep the DVD video player away from any magnetic articles such as speaker etc.

■ **Superposition**

- Please place the DVD player horizontally. Do not place a heavy object (amplifier, receiver) on it. The object may fall, causing serious

personal injury or death.

This unit should be situated away from heat source, such as amplifiers, radiators, stoves or any other units producing heat.

Condensation

Lens could be moistening in these cases.

Turn on heater shortly,

In a very wet room,

Move the player from a cold environment to a heat environment quickly.

Being moisture inside the play could operate normally. Please turn on power and wait about an hour for drying the moisture.